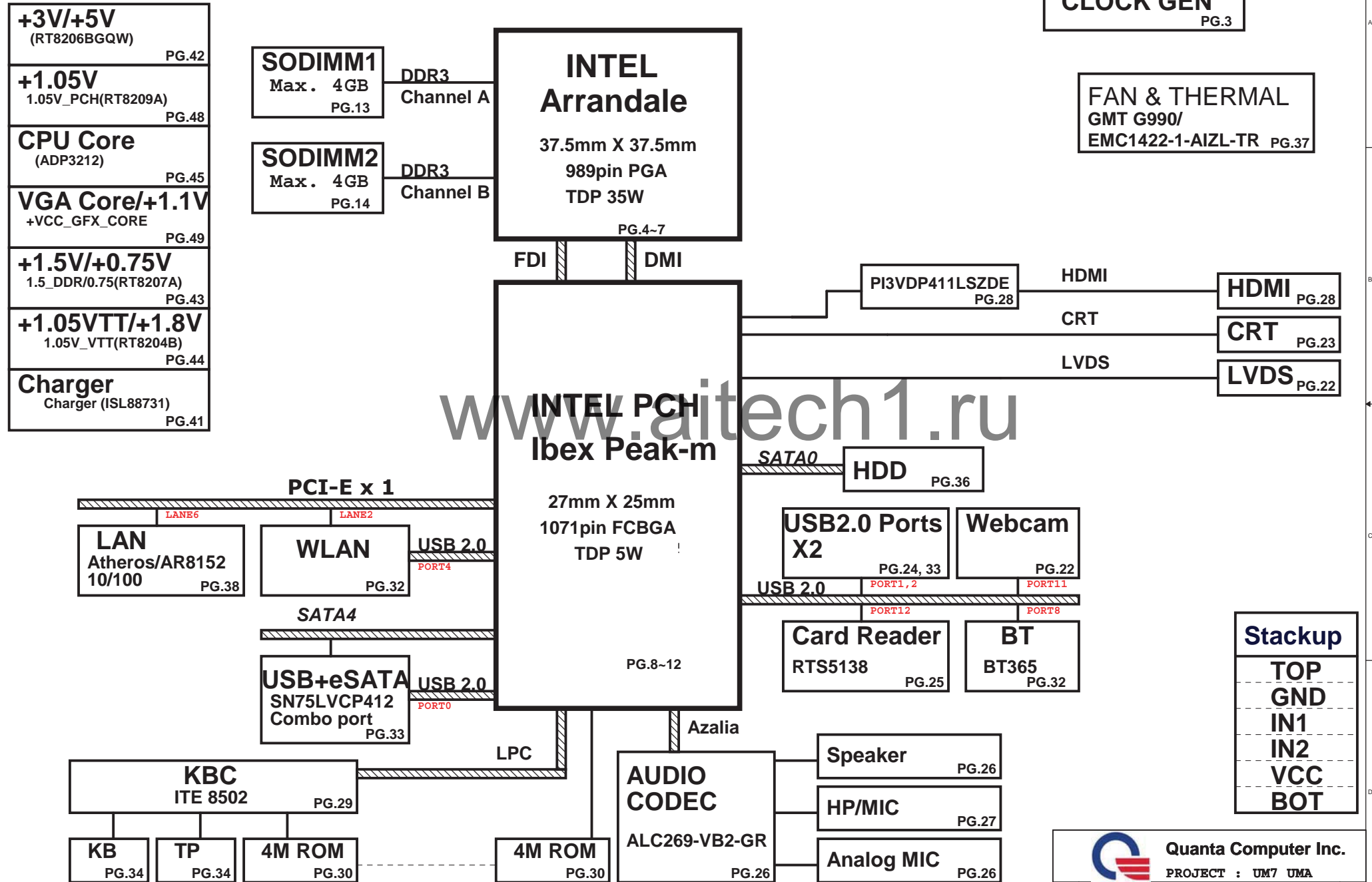


# UM7 UMA SYSTEM DIAGRAM




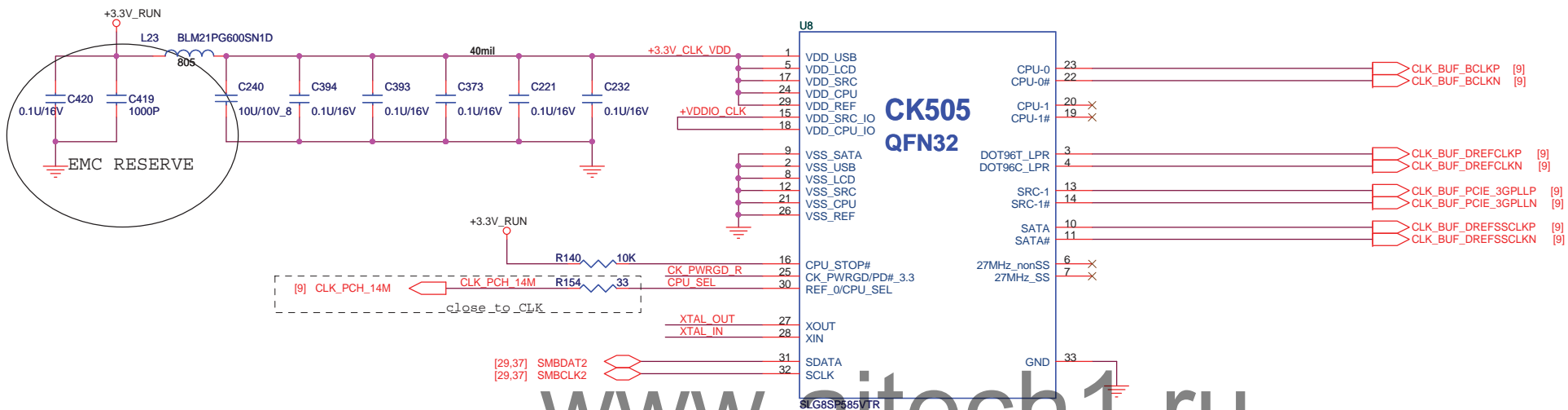
# Table of Contents

PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3	Clock Generator
4-7	PROCESSER Arrandale
8-12	PCH
13-14	DDRIII SO-DIMM(204P)
15-21	Blank Page
22	LCD CONN W/CCD
23	CRT CONN
24	Right side USB
25	Cardreader (RTS5138)
26	Azalia (ALC269)
27	Audio Connector
28	HDMI CONN
29	SIO(ITE8502)
30	FLASH / RTC
31	Blank Page
32	MINI-Card (WLAN)+BT
33	ESATA & Left USB
34	TP / KEYBOARD
35	SATA HDD
36	SWITCH LED
37	FAN / THERMAL
38	LAN(AR8152/RJ-45)
39	Blank Page
40	System Reset Circuit
41	Charger (MAX8731)
42	3V/5V (RT8206BGQW)
43	1.5_DDR/0.75(RT8207A)
44	1.05V_VTT(RT8204B)
45	CPU CORE(ADP3212)
46	Run Power Switch
47	DCin & Batt
48	1.05V_PCH(RT8209A)
49	GFX_VCORE (ADP3211)
50	Power Block Diagram
51	Power sequence Block

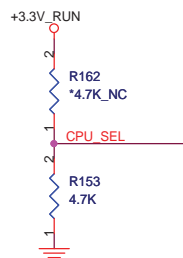
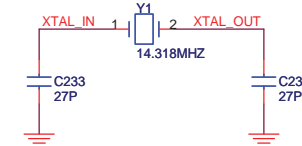
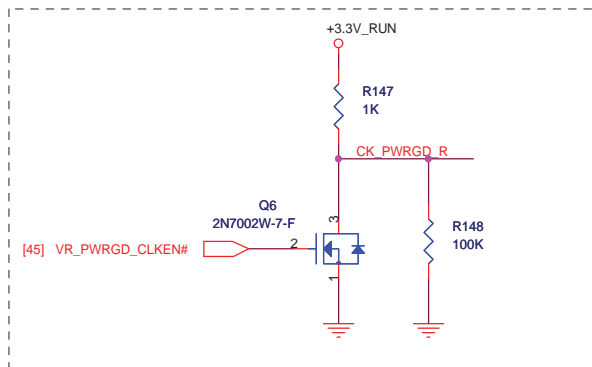
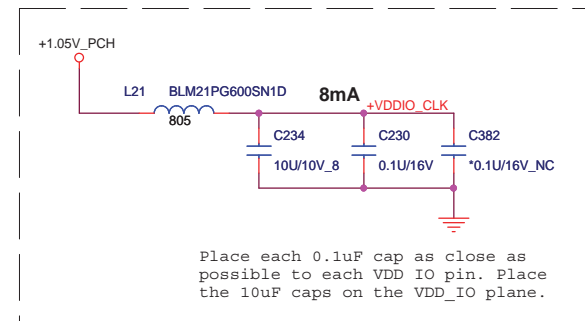
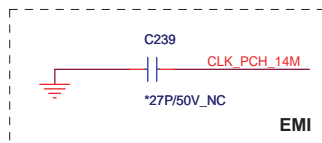
# Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	23,42,43,44,45,46,49,50	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	09,12,30,31	RTC		S0~S5
+5V_ALW	+5V	37,43,44,47,48	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	30,31,37,42,43,45,47,48	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	12,25,34,37,43,44,45,46,47,49,50	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	03,08,09,10,11,12,23,35,37,39,41,46,47,50	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	04,06,14,15,44,47	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	14,15,44	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	08,12,23,24,27,28,29,35,36,37,38,47	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,4,8,9,10,11,12,14,15,23,24,26,27,28,29,30,31,33,34,36,37,38,39,41,47	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	6,12,45	SDVO POWER	RUN_ON	
+1.05V_VTT	+1.1V	4,6,11,12,45,46	CPU POWER	RUN_ON	
+1.5V_RUN	+1.5V	12,33,47	PCH/Min Card	RUN_ON	
+1.05V_PCH	+1.05V	3,8,9,10,12,49	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	6,46	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	23	LCD Power	LCDVCC_TST_EN & ENVDD	

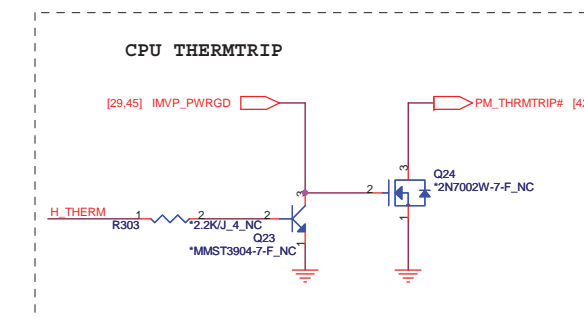
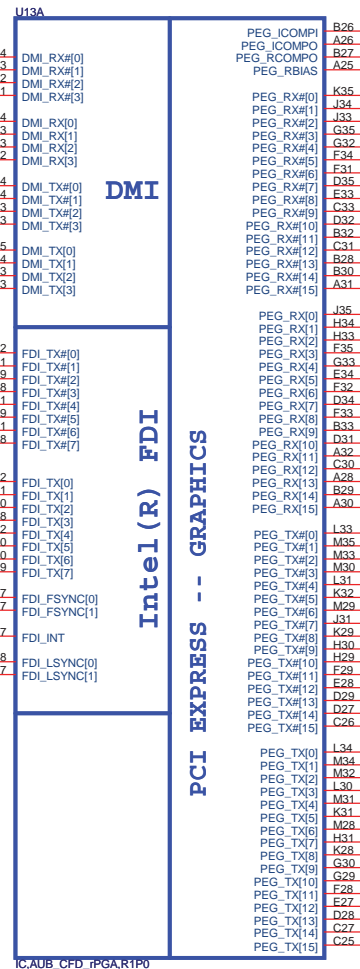
GND PLANE	PAGE	DESCRIPTION
 GND	ALL	



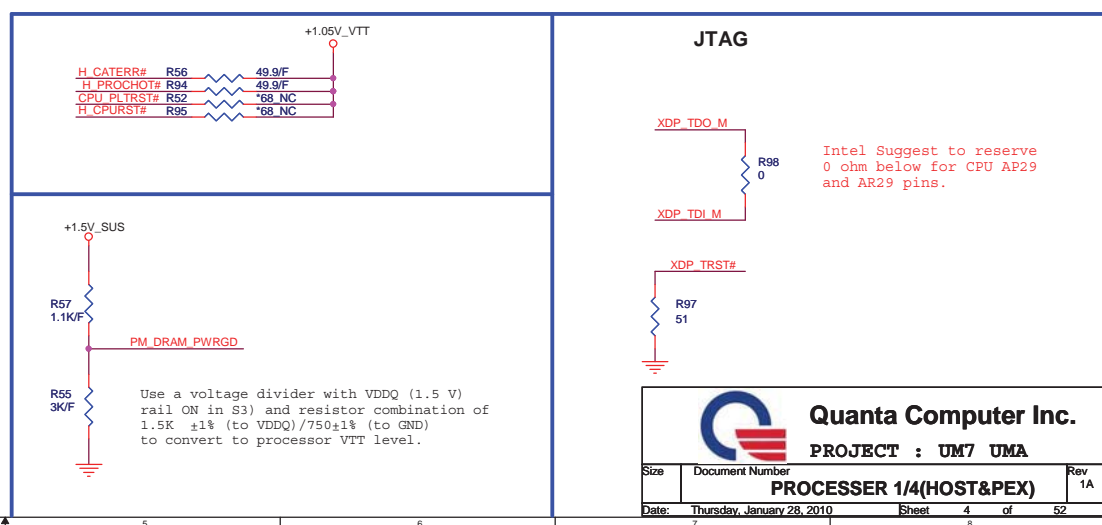
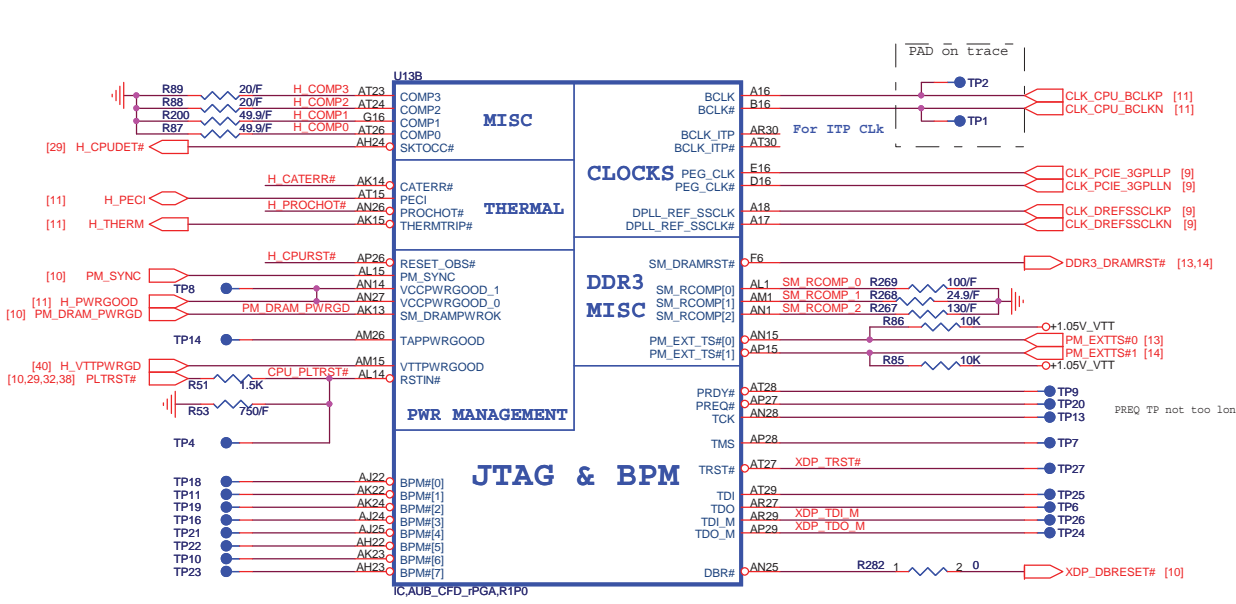
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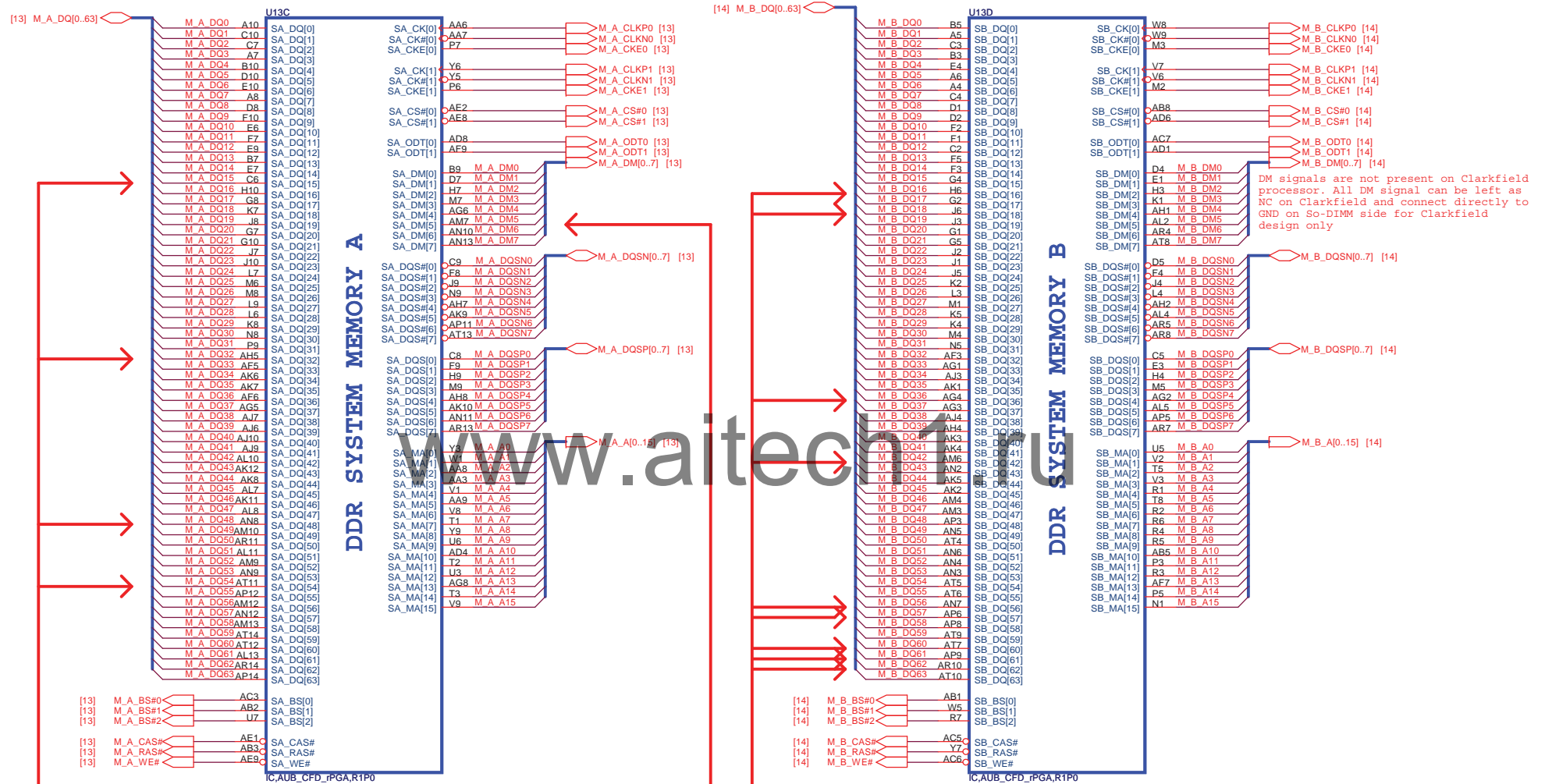
PIN 30	CPU_0	CPU_1
0 (default)	133MHz	133MHz
1 (0.7V-1.5V)	100MHz	100MHz



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# AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



**POWER**

**CPU CORE SUPPLY**

**CPU VIDS**

**SENSE LINES**

**1.1V RAIL POWER**

**1.8V**

**1.1V**

**DDR3 - 1.5V RAILS**

**GRAPHICS**

**SENSE LINES**

**GRAPHICS VIDS**

**FDI**

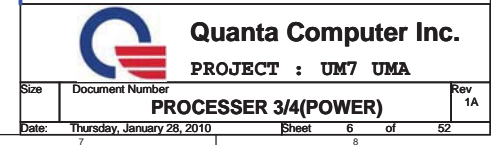
**PG & DVT**

**VTT Rail Values are**  
Auburndal VTT=1.05V  
Clarksfield VTT=1.1V

**H VTTVID1=Low, 1.1V**  
**H VTTVID1=High, 1.05V**

**VSS SENSE VTT:**  
S(VT, 0)P20  
Connect VSS SENSE\_VTT to GND  
or can be left floating.  
Note: CRB has the VSS SENSE\_VTT floating.

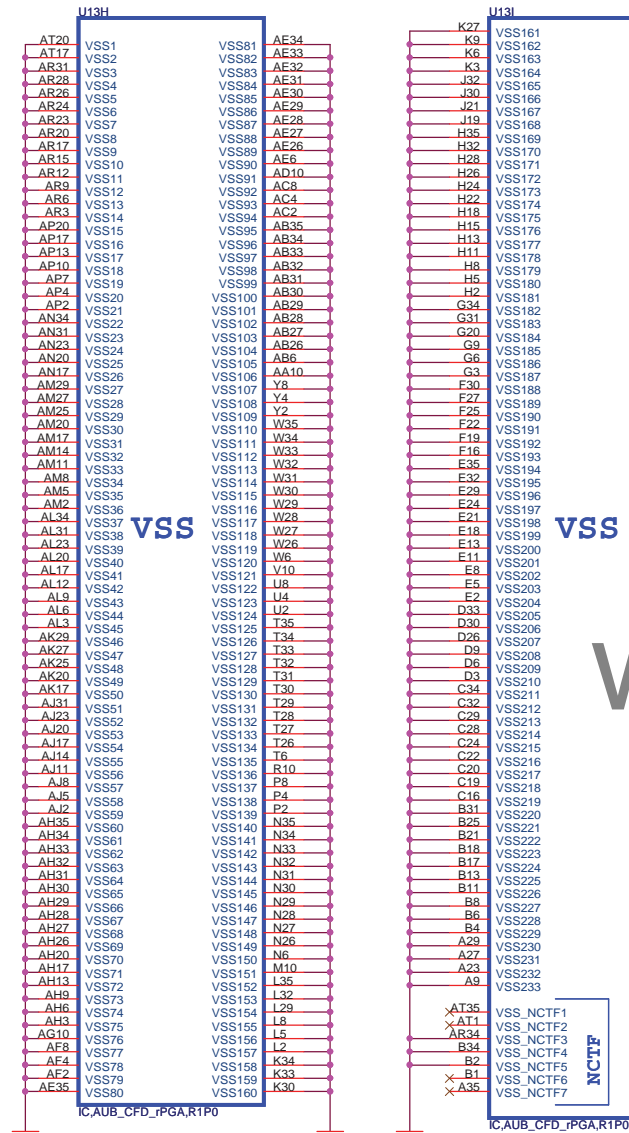
**HFM VID : Max 1.4V**  
**LFM VID : Min 0.65V**



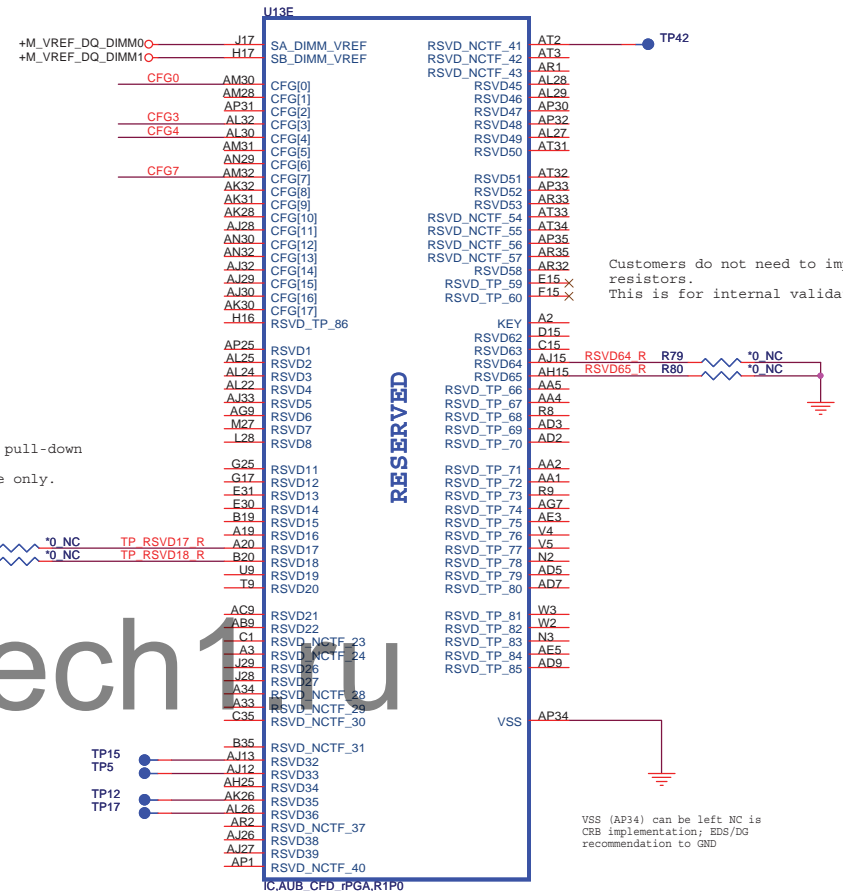


# Arrandale PROCESSOR (GND)

# Arrandale PROCESSOR( RESERVED, CFG)



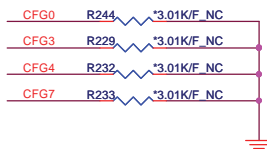
Customers do not need to implement the pull-down resistors.  
This is for internal validation purpose only.



Customers do not need to implement the pull-down resistors.  
This is for internal validation purpose only.

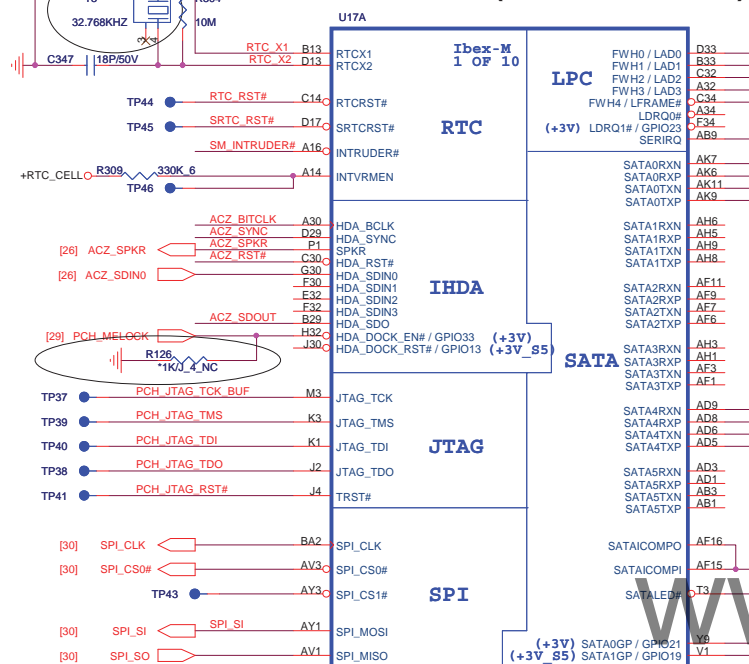
VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND

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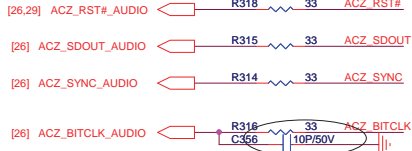
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed



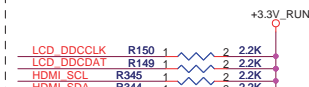
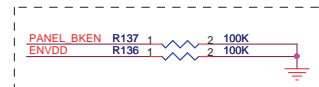
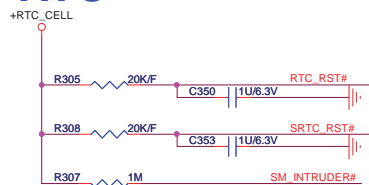
TPM Function	
Enable	Mount
Disable	NC (Default)

**For AUDIO**



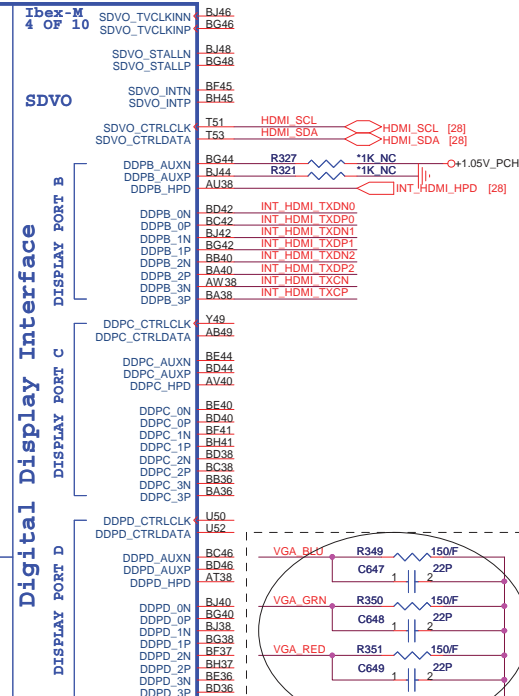
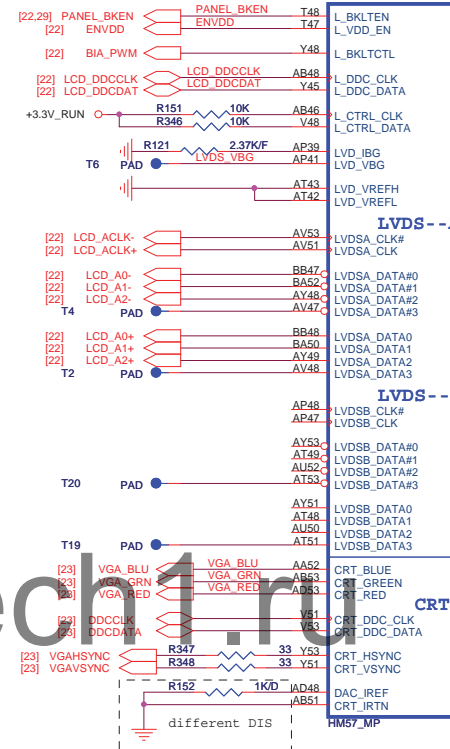
**No Reboot strap.**

SPKR	Low = Default. High = No Reboot
------	------------------------------------



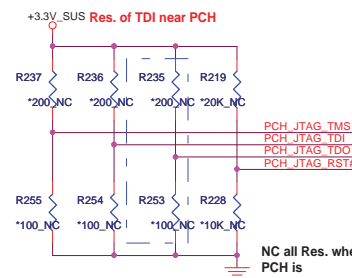
## IBEX PEAK-M (LVDS,DDI)

U17D







| Close BGA bal

**Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.**



NC all Res. when PCH is production stage.	Res. of TDO PCH ES1 stage : NC PCH ES2 stage : pop
---	--

### For UMA HDMI Function

INT_HDMI_TXD0	C334	0.1U/16V		INT_HDMI_TXD2	C28
INT_HDMI_TXDP0	C337	0.1U/16V		INT_HDMI_TXDP2	C28
INT_HDMI_TXD1	C329	0.1U/16V		INT_HDMI_TXD1	C28
INT_HDMI_TXDP1	C331	0.1U/16V		INT_HDMI_TXDP1	C28
INT_HDMI_TXD2	C334	0.1U/16V		INT_HDMI_TXD0	C28
INT_HDMI_TXDP2	C327	0.1U/16V		INT_HDMI_TXDP0	C28
INT_HDMI_TXCN	C320	0.1U/16V		INT_HDMI_TXCN	C28
INT_HDMI_TXCP	C323	0.1U/16V		INT_HDMI_TXCR	C28



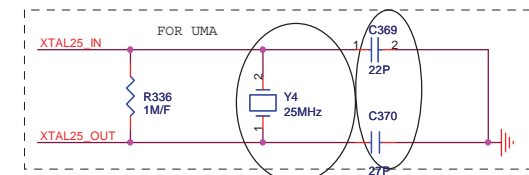
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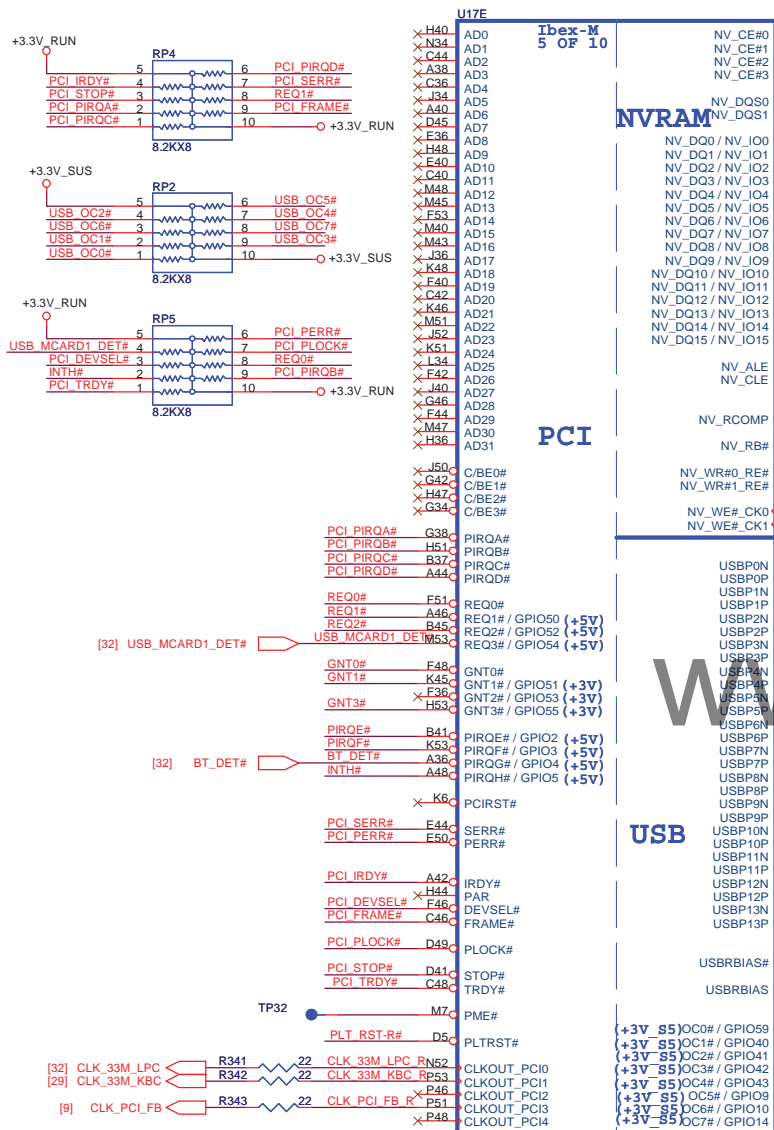
Size	Document Number	Rev
	<b>PCH 1/5 (SATA,HDA,LPC)</b>	1/
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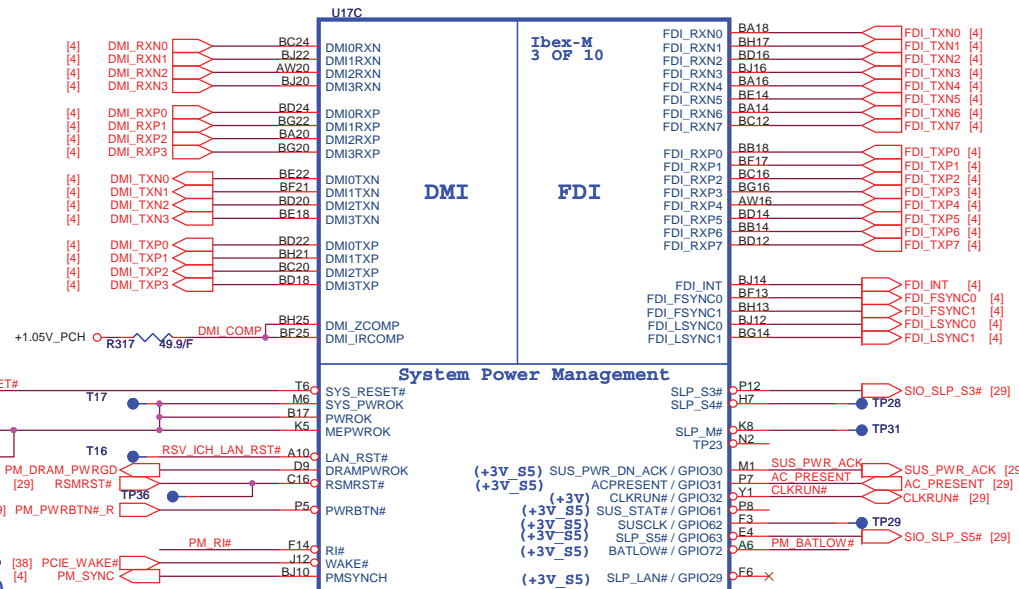
A171	VSS159	VSS259	H49
B11	VSS160	VSS260	H5
B15	VSS161	VSS261	J24
B19	VSS162	VSS262	K11
B23	VSS163	VSS263	K43
B31	VSS164	VSS264	K7
B35	VSS165	VSS265	L14
B39	VSS166	VSS266	L47
B43	VSS167	VSS267	L18
B47	VSS168	VSS268	L2
B7	VSS169	VSS269	L26
B12	VSS170	VSS270	L32
B16	VSS171	VSS271	L40
B20	VSS172	VSS272	L52
B24	VSS173	VSS273	M12
B28	VSS174	VSS274	M16
B30	VSS175	VSS275	M20
B34	VSS176	VSS276	M38
B38	VSS177	VSS277	M34
B49	VSS178	VSS278	M38
B53	VSS179	VSS279	M42
B55	VSS180	VSS280	M46
BC10	VSS181	VSS281	M49
BC14	VSS182	VSS282	M5
BC18	VSS183	VSS283	M8
BC22	VSS184	VSS284	N24
BC32	VSS185	VSS285	P11
BC36	VSS187	VSS287	AD15
BC40	VSS188	VSS288	P22
BC44	VSS189	VSS289	P20
B42	VSS190	VSS290	P32
BH9	VSS191	VSS291	P34
BD48	VSS192	VSS292	P42
BD49	VSS193	VSS293	P45
BD5	VSS194	VSS294	P47
BE12	VSS195	VSS295	R2
BE16	VSS196	VSS296	R12
BE20	VSS197	VSS297	T46
BE24	VSS198	VSS298	T41
BE30	VSS199	VSS299	T46
BE34	VSS200	VSS300	T49
BE38	VSS201	VSS301	T5
BE42	VSS202	VSS302	T8
BE46	VSS203	VSS303	U30
BE48	VSS204	VSS304	U31
BE50	VSS205	VSS305	U32
BE6	VSS206	VSS306	U34
BE8	VSS207	VSS307	P38
BF3	VSS208	VSS308	V11
BF6	VSS209	VSS309	V19
BF51	VSS210	VSS310	V20
BG18	VSS211	VSS311	V12
BG24	VSS212	VSS312	V22
BG4	VSS213	VSS313	V30
BG50	VSS214	VSS314	V31
BH11	VSS215	VSS315	V32
BH15	VSS216	VSS316	V35
BH19	VSS217	VSS317	V38
BH23	VSS218	VSS318	V43
BH31	VSS219	VSS319	V45
BH35	VSS220	VSS320	V46
BH39	VSS221	VSS321	V47
BH43	VSS222	VSS322	V49
BH47	VSS223	VSS323	V5
BH7	VSS224	VSS324	V7
C12	VSS225	VSS325	V8
C50	VSS226	VSS326	V8
D51	VSS227	VSS327	W2
E12	VSS228	VSS328	Y11
E16	VSS229	VSS329	Y12
E20	VSS230	VSS330	Y15
E24	VSS231	VSS331	Y19
E30	VSS232	VSS332	Y23
E34	VSS233	VSS333	Y28
E38	VSS234	VSS334	Y30
E42	VSS235	VSS335	Y31
E46	VSS236	VSS336	Y32
E48	VSS237	VSS337	Y33
E6	VSS238	VSS338	Y38
E8	VSS239	VSS339	Y43
F49	VSS240	VSS340	Y46
F5	VSS241	VSS341	Y5
G10	VSS242	VSS342	Y6
G14	VSS243	VSS343	Y8
G18	VSS244	VSS344	Y8
G2	VSS245	VSS345	T24
G22	VSS246	VSS346	P43
G32	VSS247	VSS347	AD51
G36	VSS248	VSS348	AT8
G40	VSS249	VSS349	AD47
G44	VSS250	VSS350	Y47
G52	VSS251	VSS351	AT12
AF39	VSS252	VSS352	AT16
H16	VSS253	VSS353	AM3
H20	VSS254	VSS354	AM5
H30	VSS255	VSS355	AK45
H34	VSS256	VSS356	AK39
H38	VSS257	VSS357	AV14
H42	VSS258		



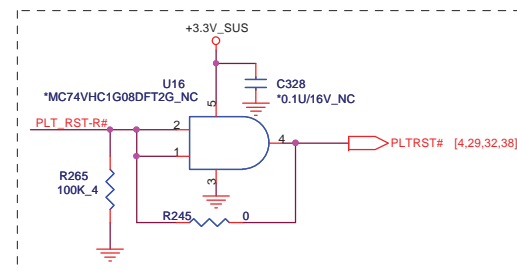
# IBEX PEAK-M (PCI,USB,NVRAM)



# IBEX PEAK-M (DMI,FDI,GPIO)



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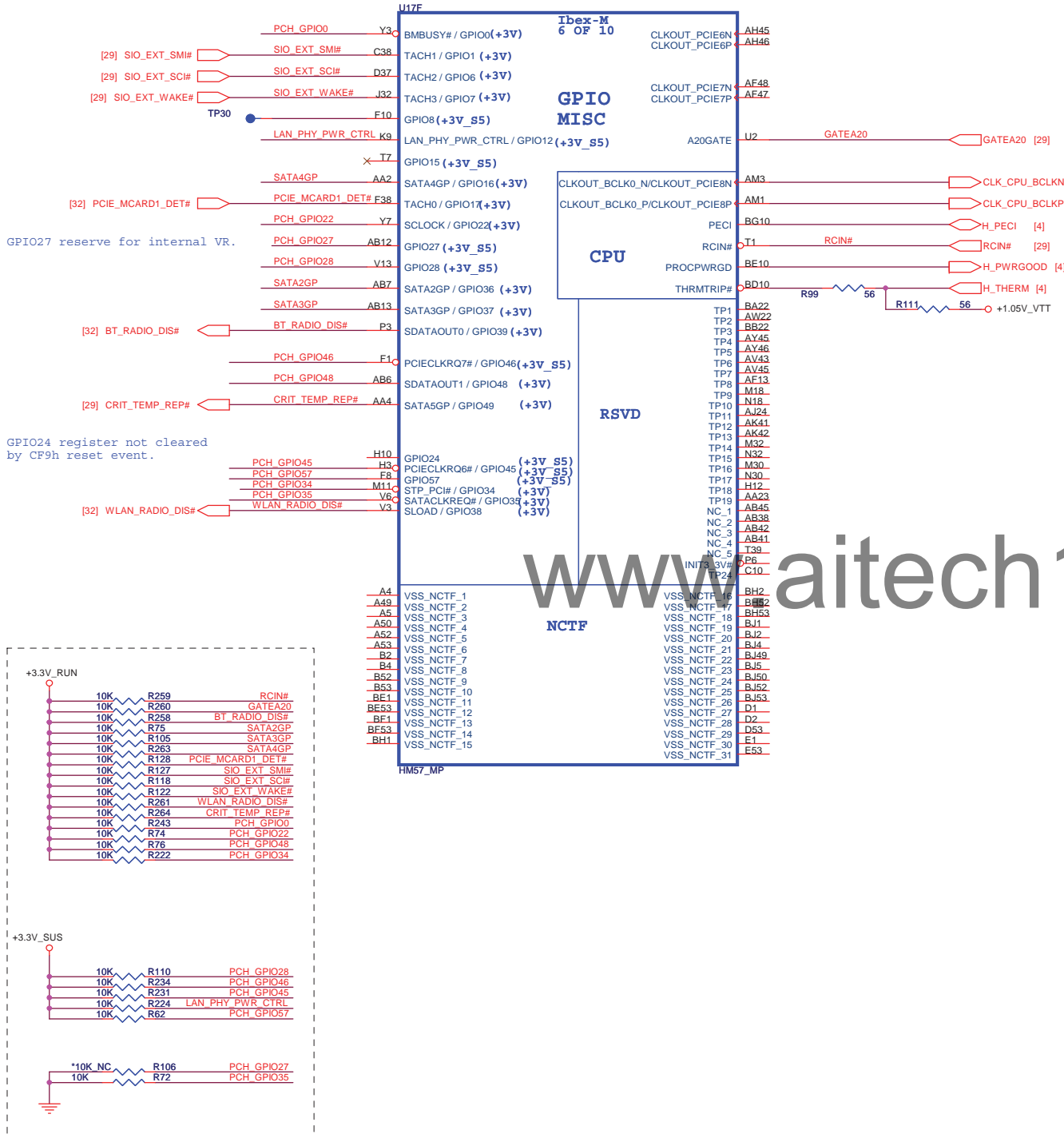


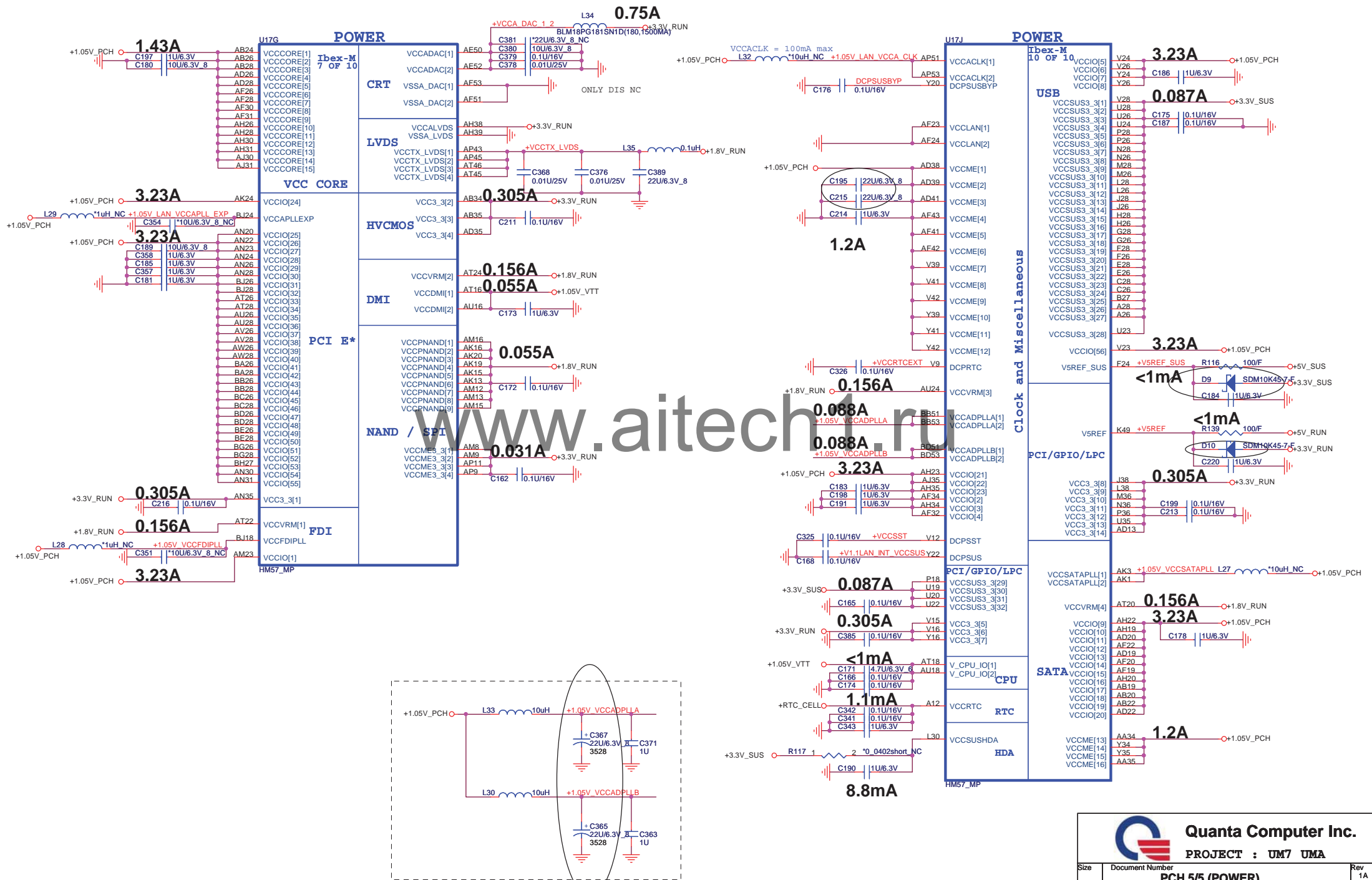
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# IBEX PEAK-M (GPIO,VSS\_NCTF,RSVD)

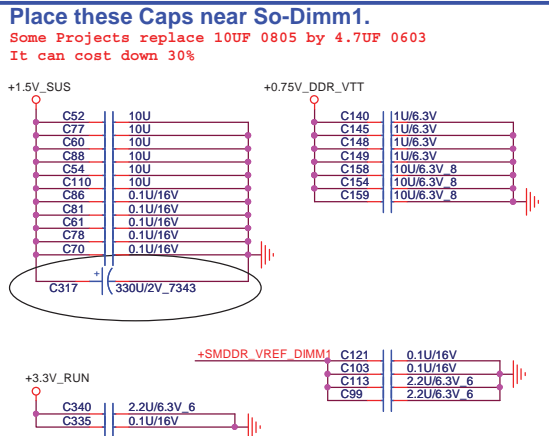
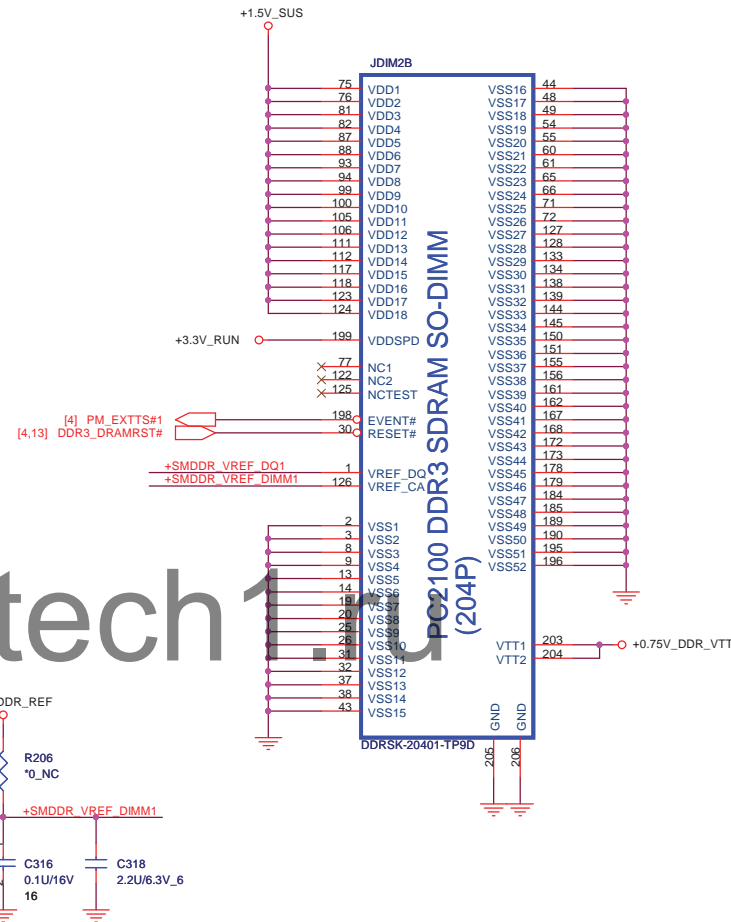
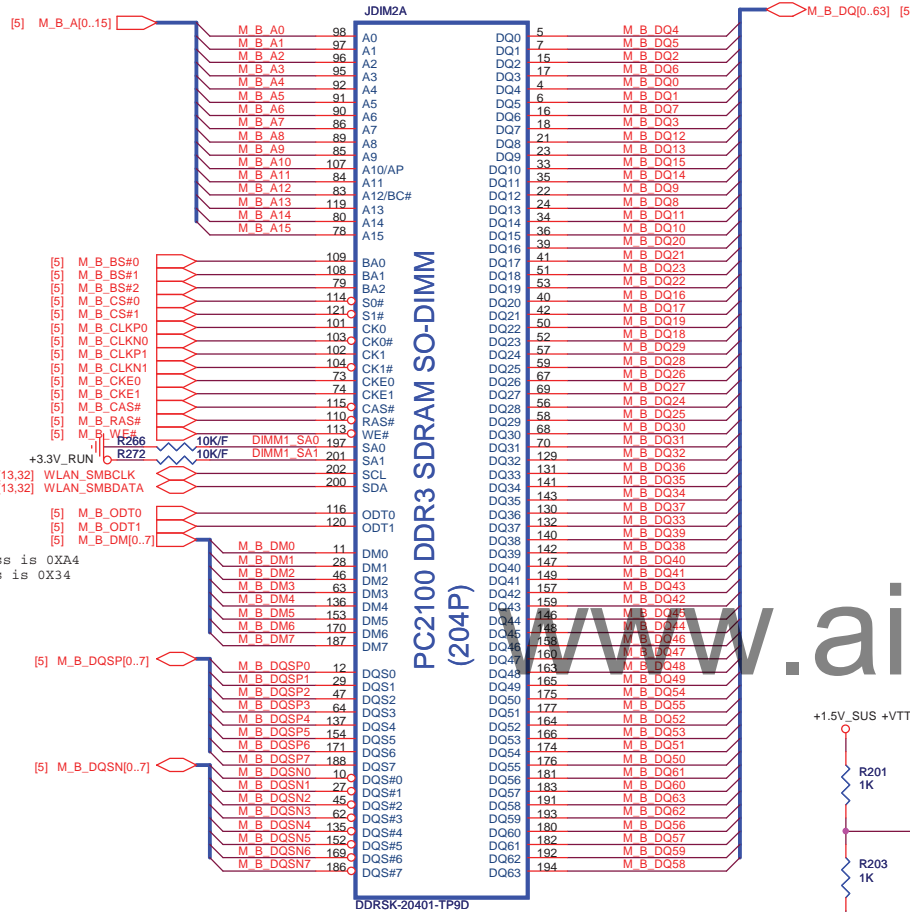
# IBEX PEAK-M (GND)



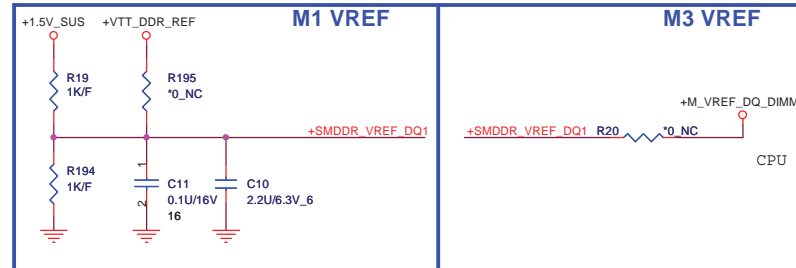









H9.2



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		<b>PROJECT : UM7 UMA</b>	
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	<b>Blank</b>	1A
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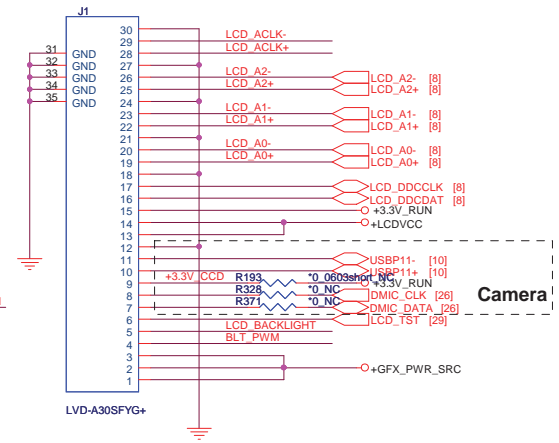
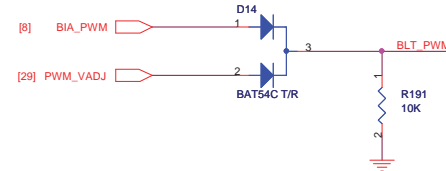
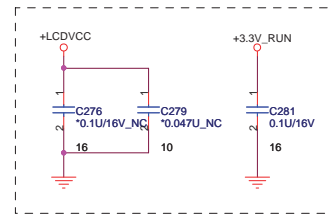
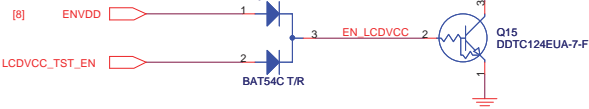


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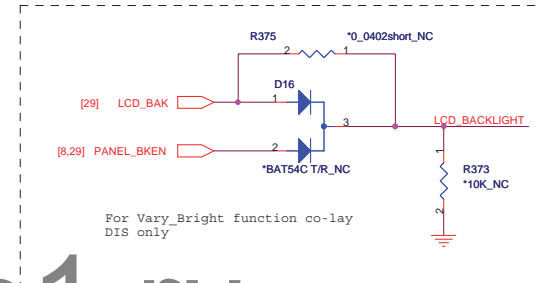
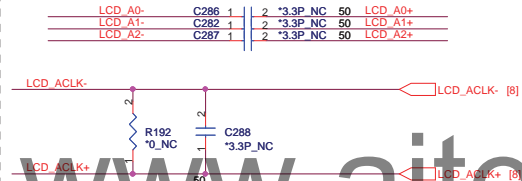
**PROJECT : UM7 UMA**

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	<b>Blank</b>	1A
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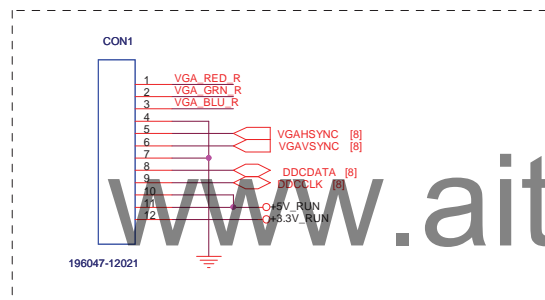
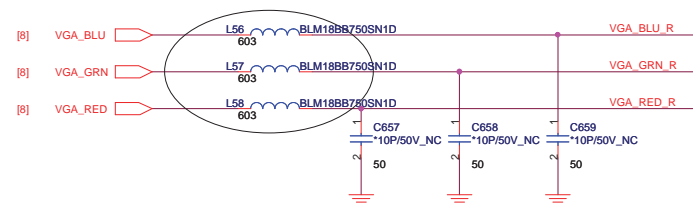
Support the new imbedded diagnostics.

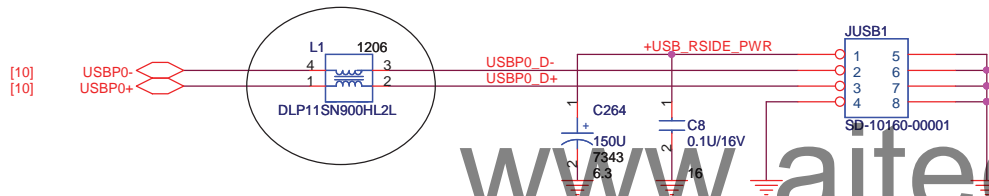
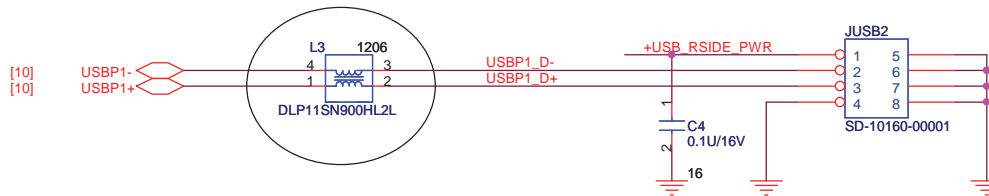


Shunt capacitors on LVDS for improving WWAN.



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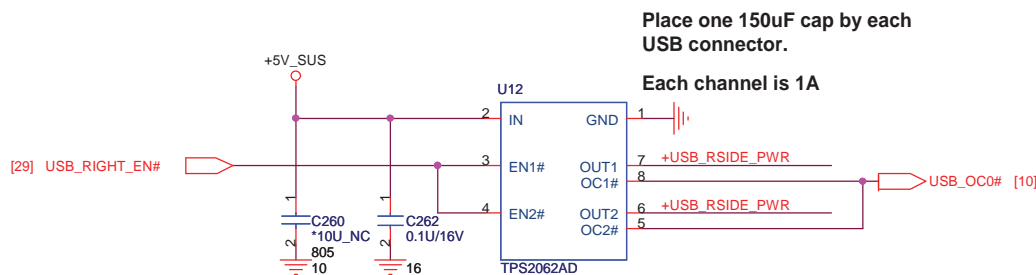
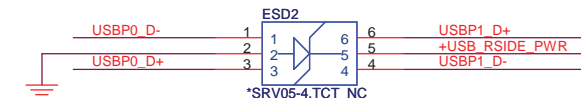




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Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.



Place one 150uF cap by each USB connector.

Each channel is 1A

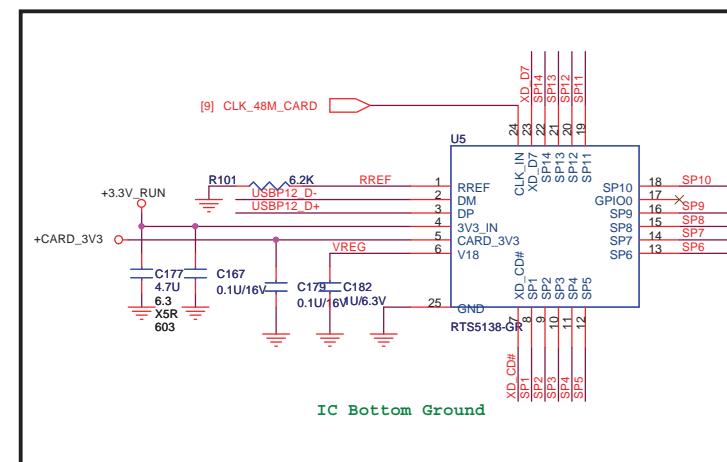
<http://hobi-elektronika.net>



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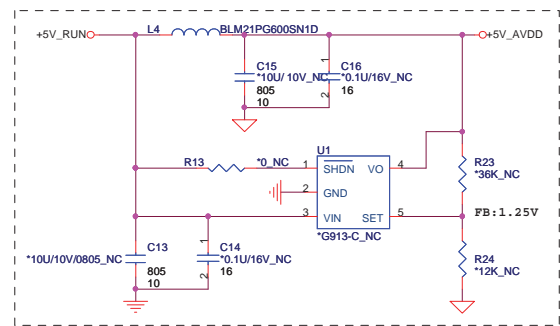
PROJECT : UM7 UMA

Size	Document Number	Rev
	Right USB	1A
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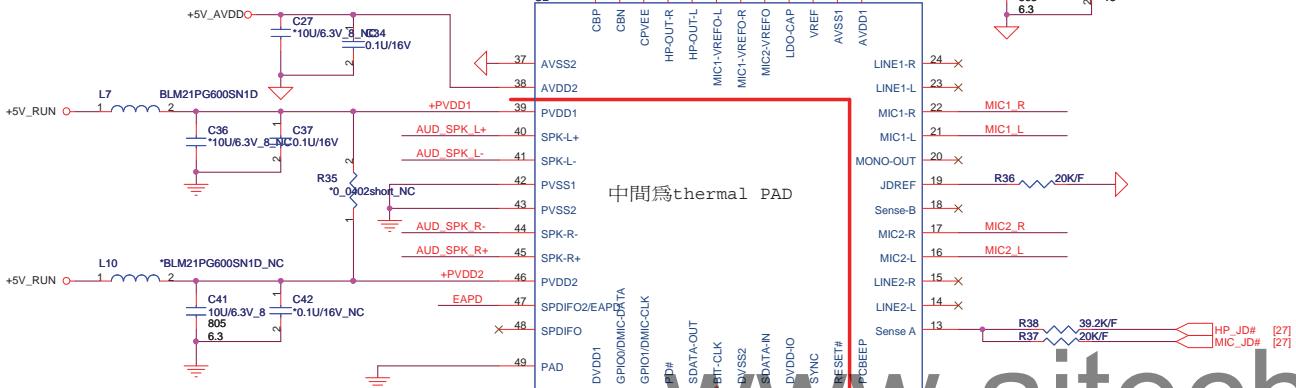


IC Bottom Ground

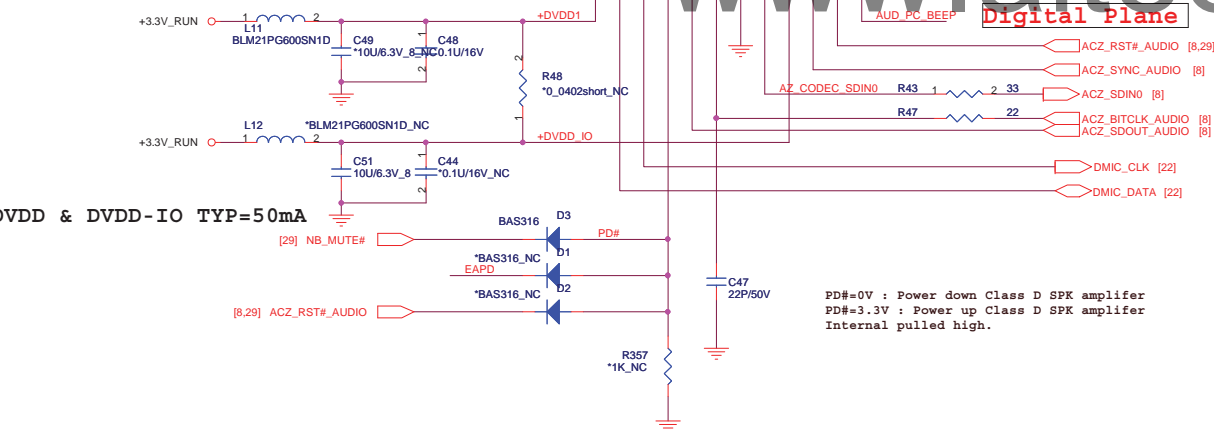
www.aitech1.ru



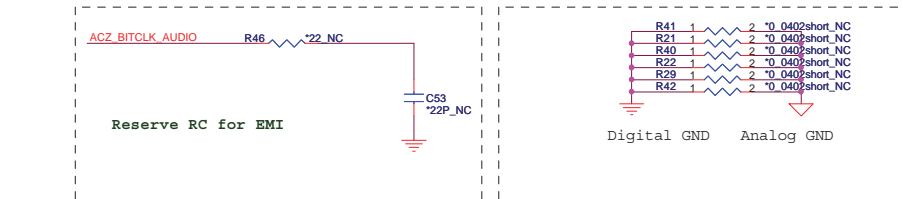
AVDD1, AVDD2 TYP=48mA



中間為thermal PAD

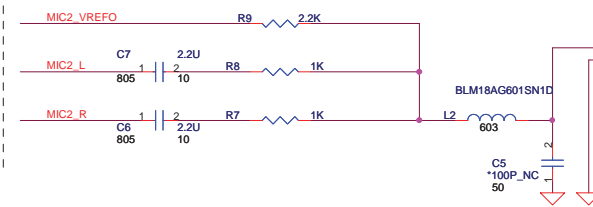


DVDD & DVDD-IO TYP=50mA

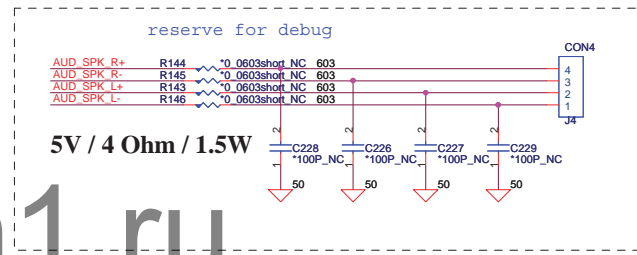


Reserve RC for EMI

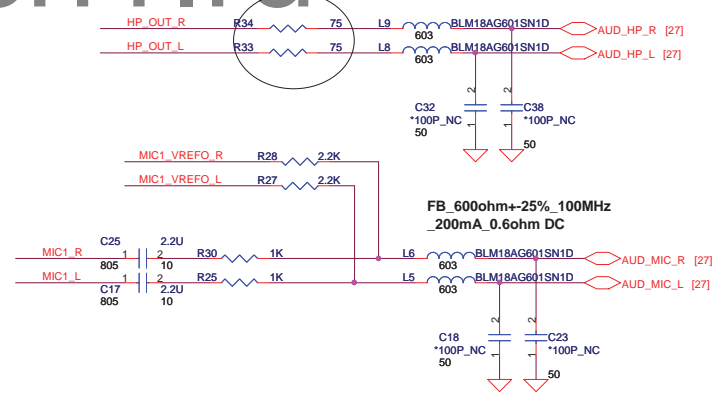
Digital GND Analog GND



<http://hobi-elektronika.net>



5V / 4 Ohm / 1.5W

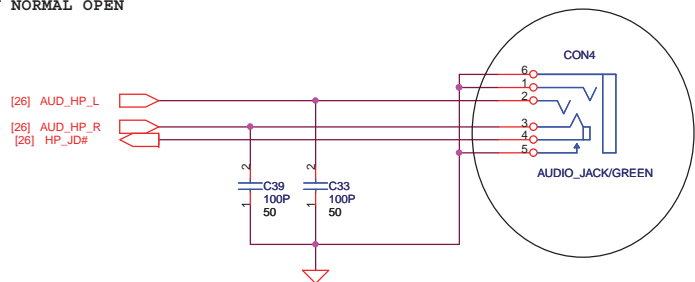


FB\_600ohm+-25%\_100MHz  
\_200mA\_0.6ohm DC



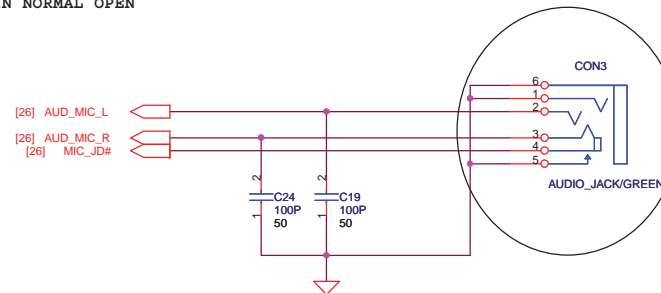
## HP JACKN

SUYIN NORMAL OPEN



## MIC JACK

SUYIN NORMAL OPEN



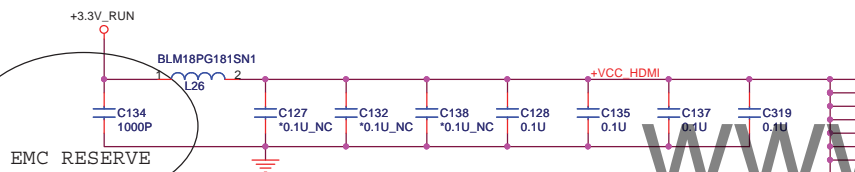
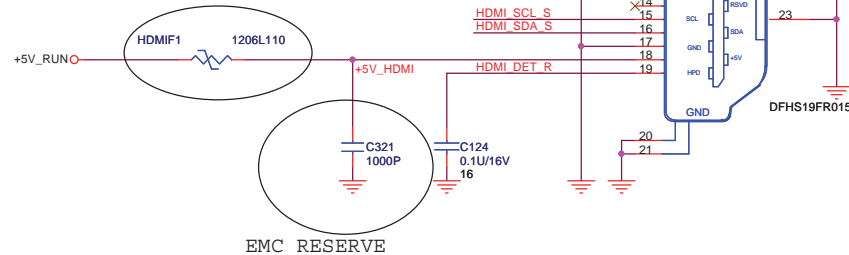
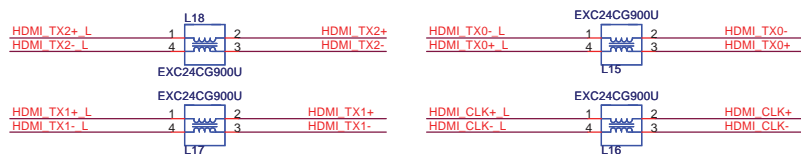
[www.aitech1.ru](http://www.aitech1.ru)



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PROJECT : UM7 UMA

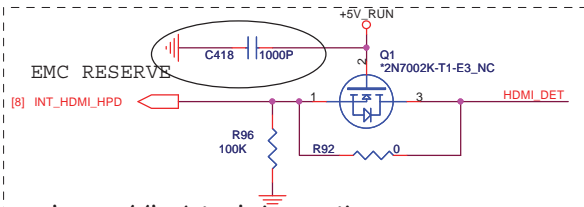
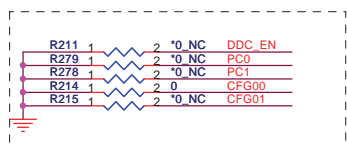
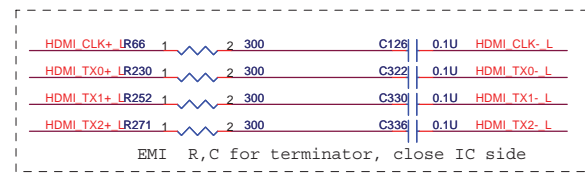
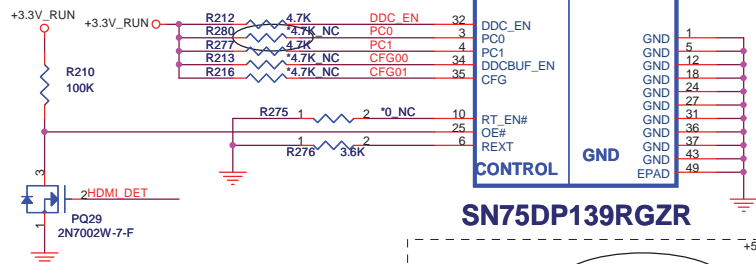
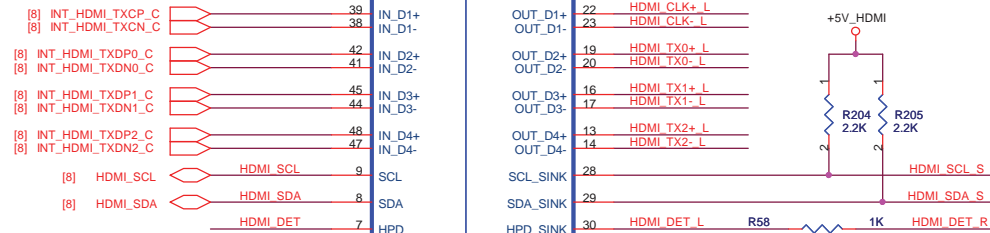
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	AUDIO CONN	1A
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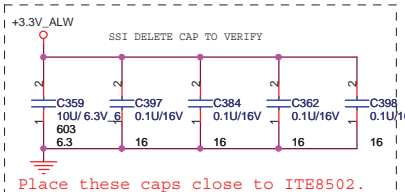
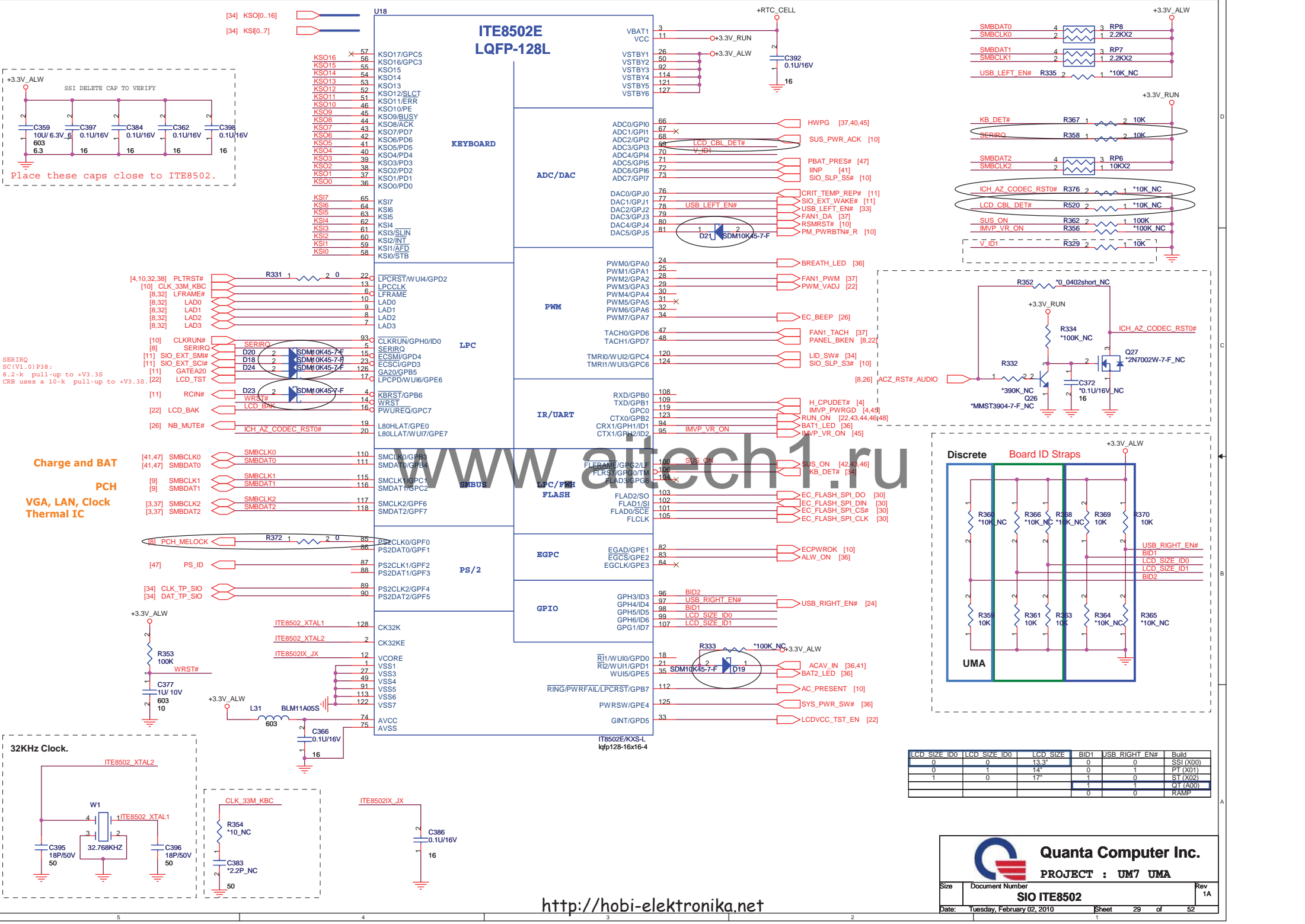


**EQUALIZATION SETTING**  
 PC1:PC0=0:0 8dB  
 PC1:PC0=0:1 4dB Recommended  
 PC1:PC0=1:0 12dB  
 PC1:PC0=1:1 0dB

**SCL/SDA Low-level input/output Voltage**  
 CFG01:CFG00=0:0 VIL:<0.4V VOL:0.6V (Default)  
 CGF01:CGF00=0:1 VIL:<0.36V VOL:0.55V  
 CGF01:CGF00=1:0 VIL:<0.44V VOL:0.65V  
 CGF01:CGF00=1:1 VIL:<0.36V VOL:0.6V

**HDMI\_PWR\_CTRL**  
 0 is Enable  
 1 is Disable

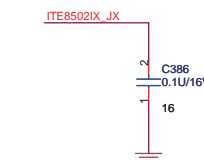
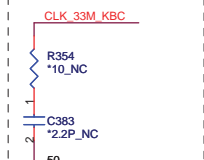
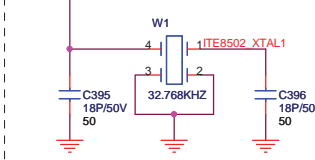




SERIRQ  
SC(V1.0)P38:  
8.2-k pull-up to +V3.3S  
CRB uses a 10-k pull-up to +V3.3S.

Charge and BAT  
PCH  
VGA, LAN, Clock  
Thermal IC

32KHz Clock.



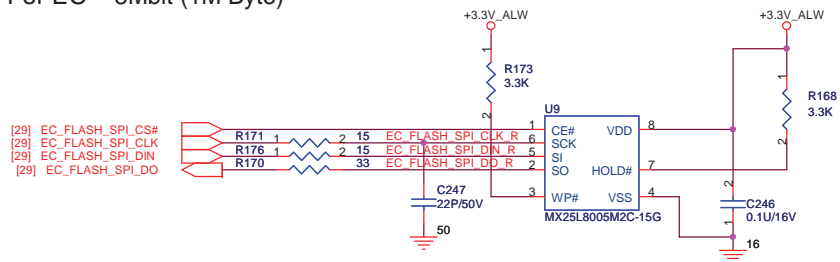
LCD SIZE ID0	LCD SIZE ID0	LCD SIZE	BID1	USB RIGHT EN#	Build
0	0	13.3"	0	0	SSI (X00)
0	1	14"	0	1	PT (X01)
1	0	17"	1	0	ST (X02)
			1	1	QT (A00)
			0	0	RAMP

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**PROJECT : UM7 UMA**  
**SIO ITE8502**

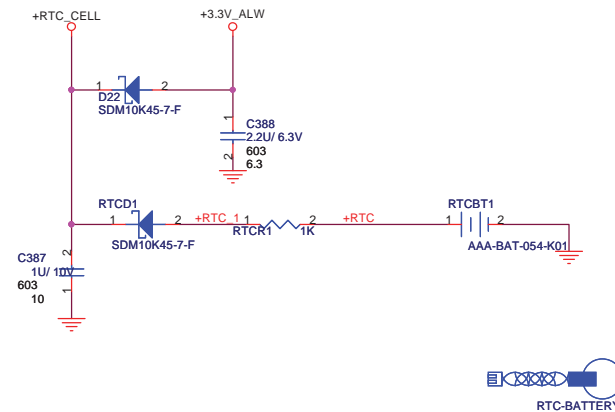
Size	Document Number	Rev
		1A

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For EC 8Mbit (1M Byte)



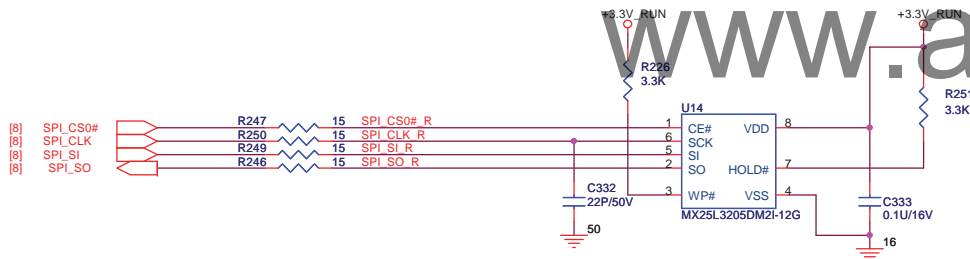
RTC BATTERY



For PCH

32Mbit (4M Byte)

2nd source:AKE39ZP0N00



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<http://hobi-elektronika.net>

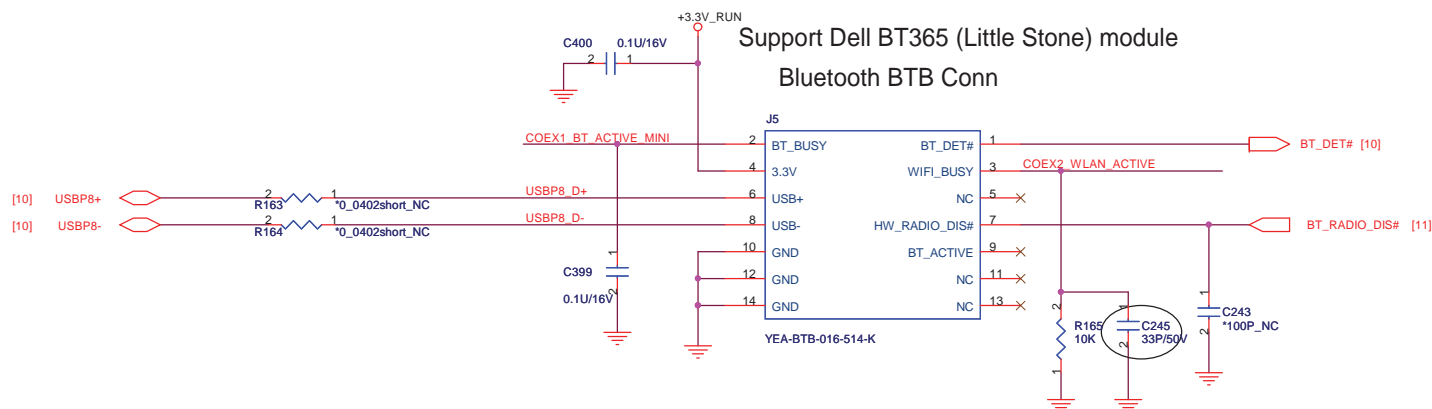
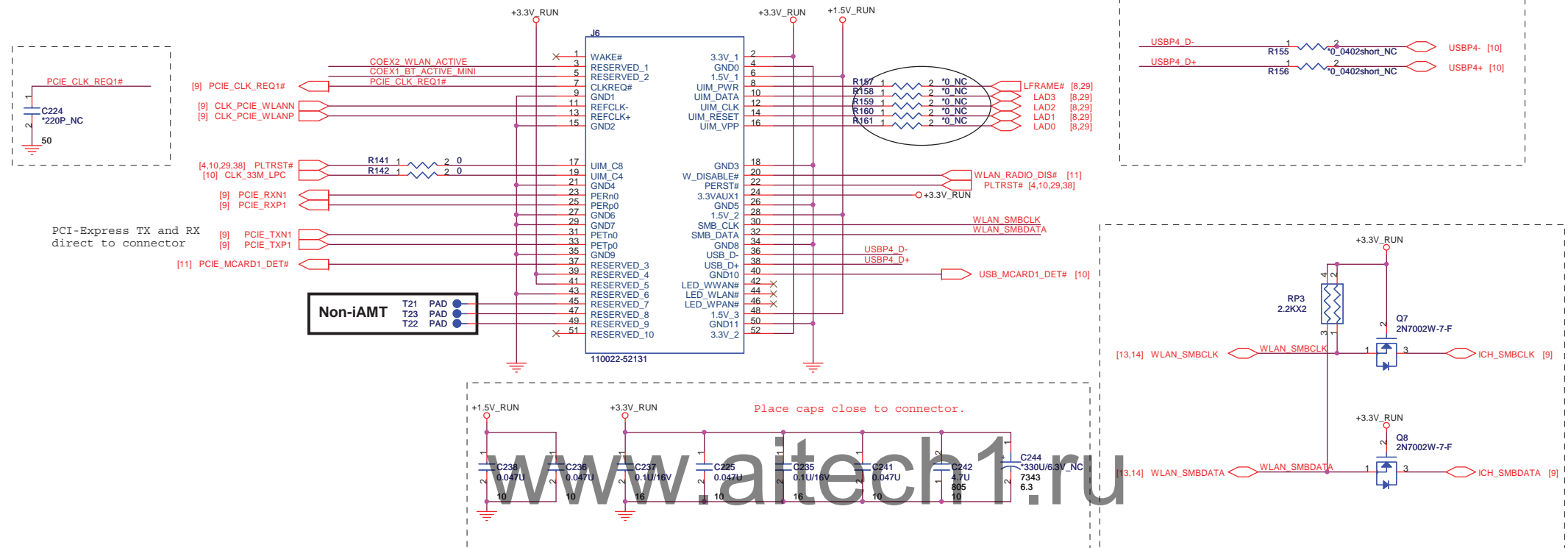


**Quanta Computer Inc.**

**PROJECT : UM7 UMA**

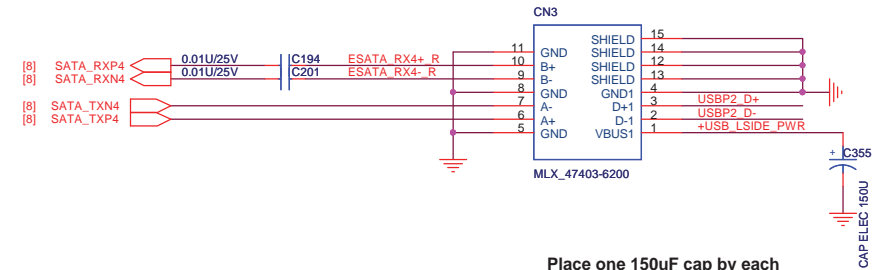
Size	Document Number	Rev
	<b>MINI-Card WWAN</b>	1A
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## MiniCard WLAN connector



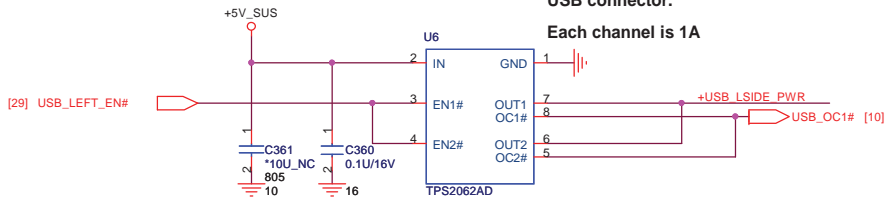


USB and eSATA Conn.

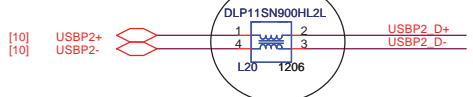


Place one 150uF cap by each USB connector.

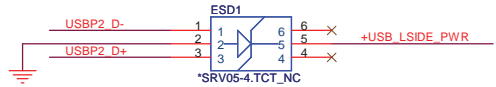
Each channel is 1A



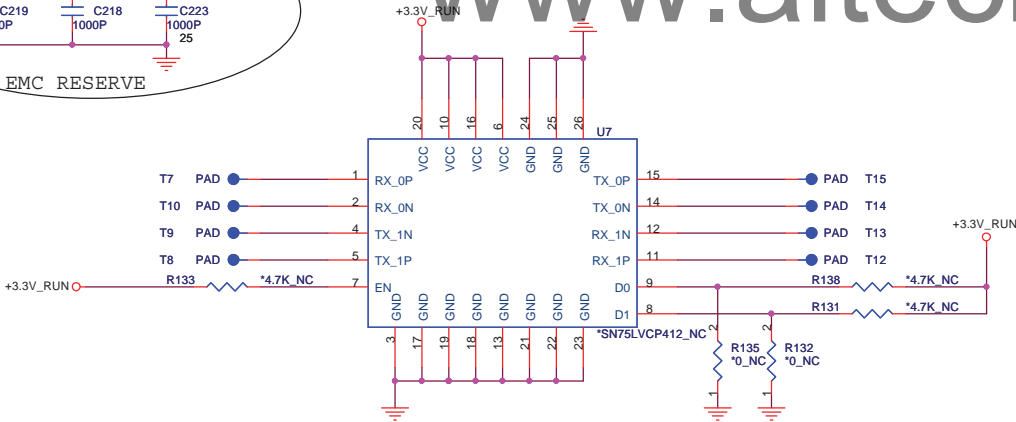
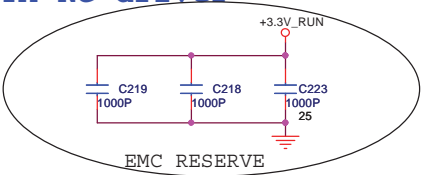
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NQPOP.



Place ESD diodes as close as USB connector.

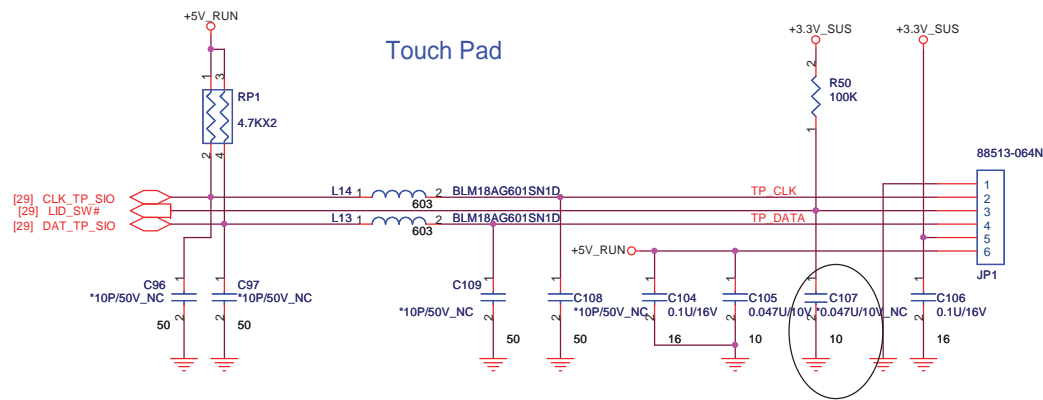


E-SATA Re-driver



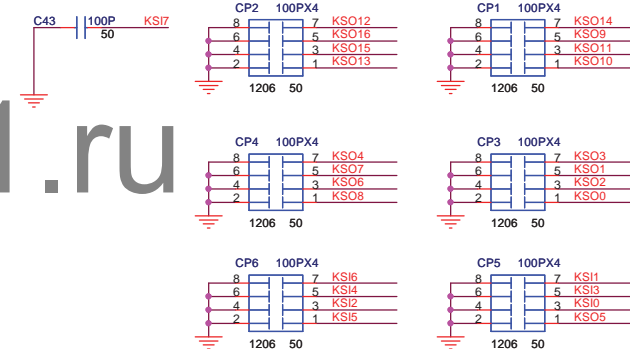
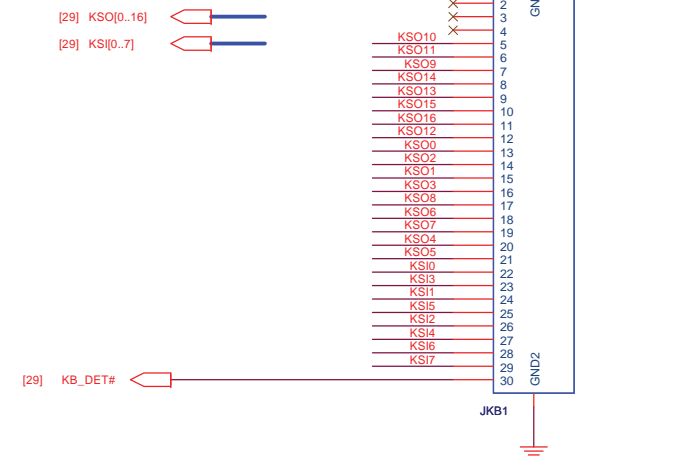
Note: Boost:5dB, Standard SATA:0dB

EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost



## KEYBOARD CONNECTOR

Top side



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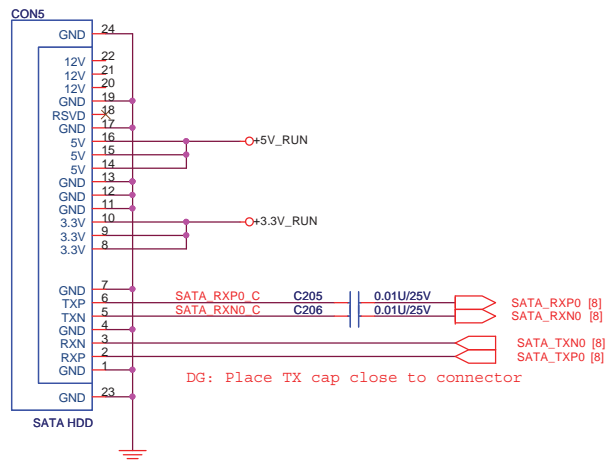


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PROJECT : UM7 UMA

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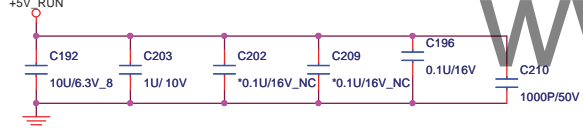
# SATA Connector.



+3.3V\_RUN Place caps close to connector.

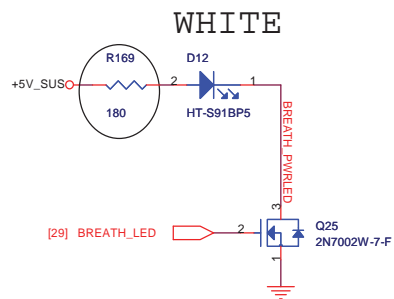


+5V\_RUN Place caps close to connector.

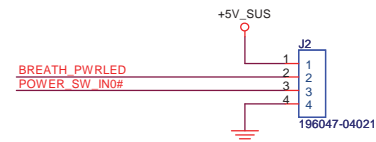


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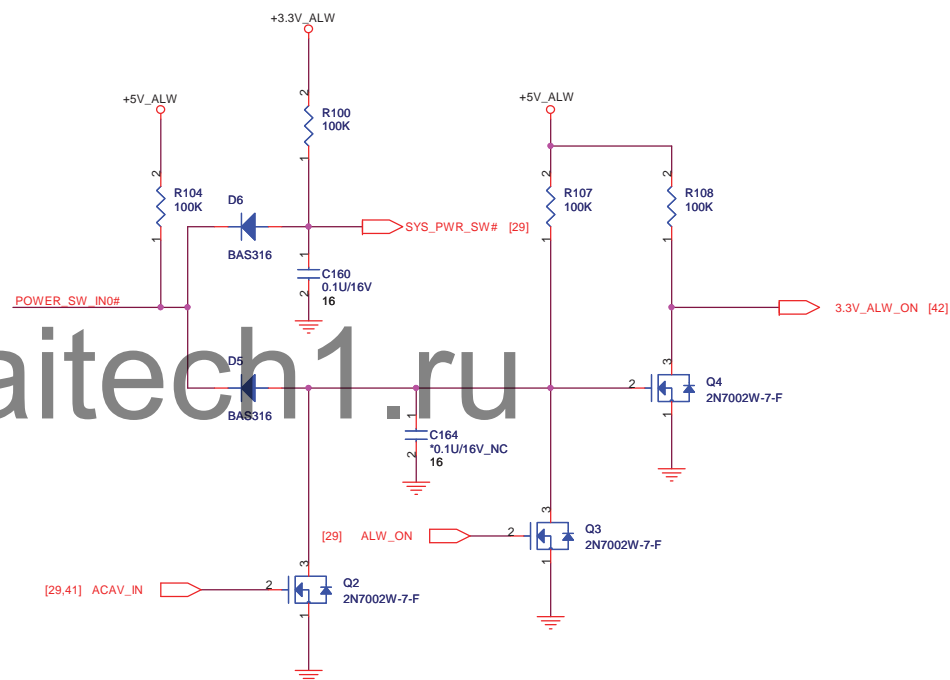
## Power



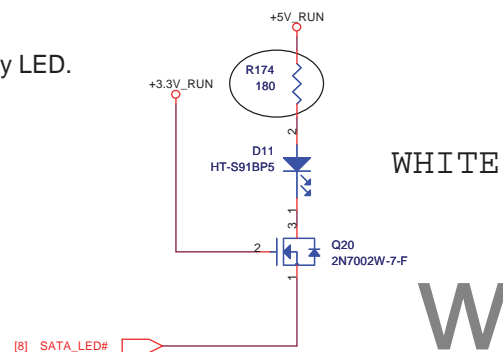
## Power button Cable



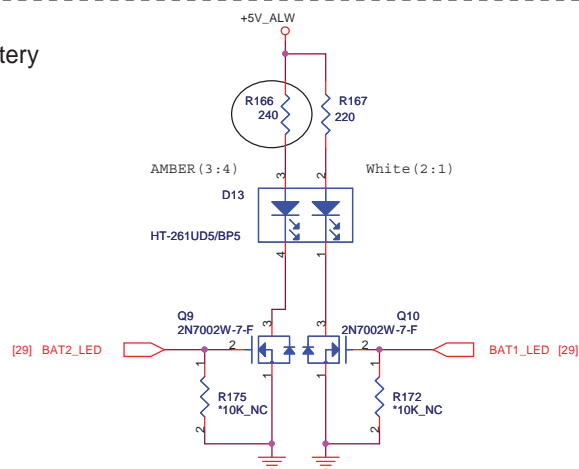
## 3VALW ON POWER LOGIC



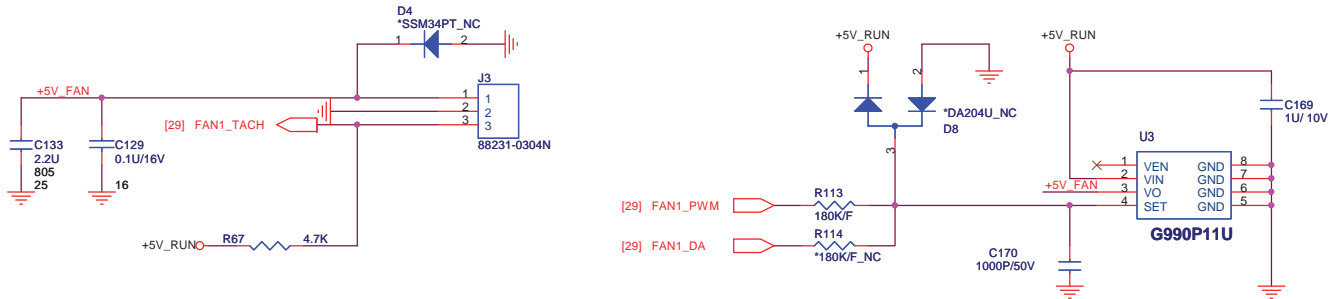
## HDD activity LED.



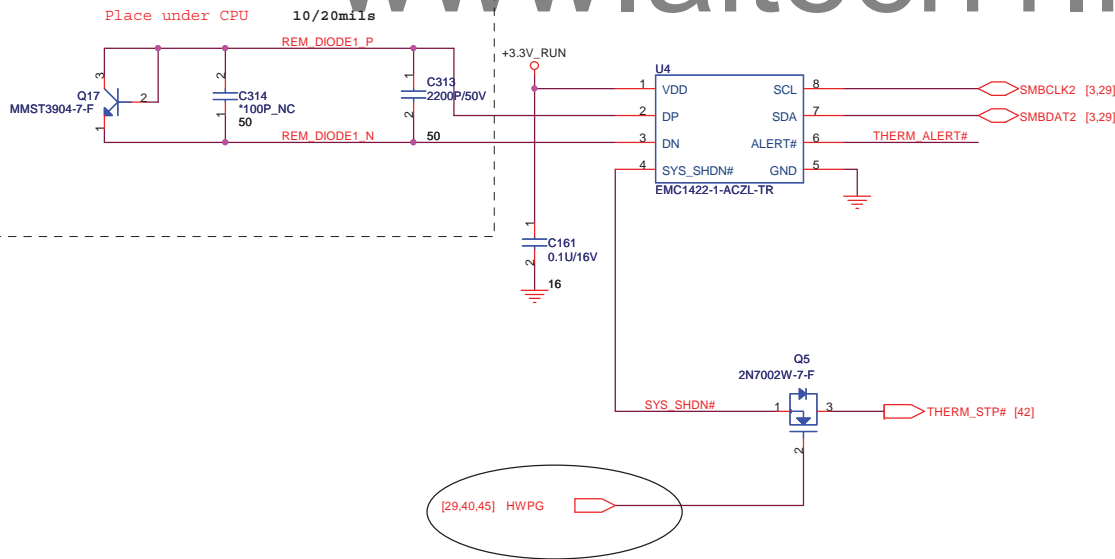
## Battery



## FAN CONTROL

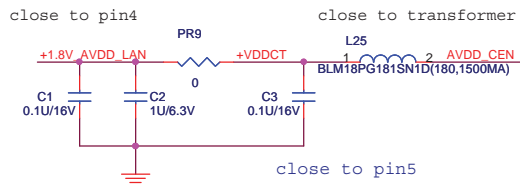
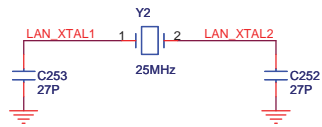


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OTP 85 degree C

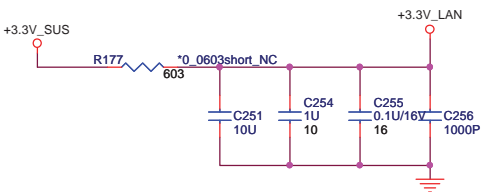
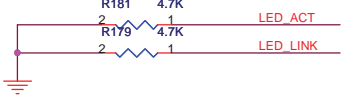




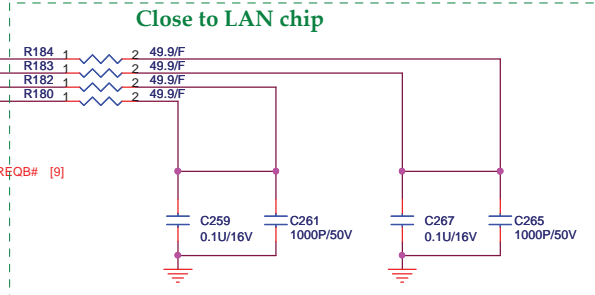
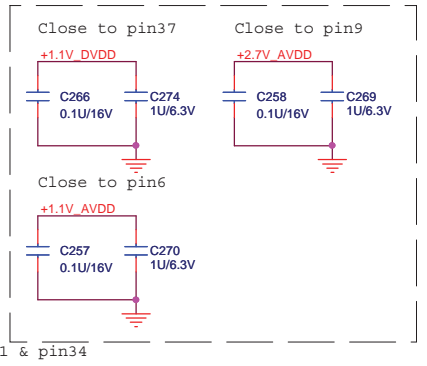
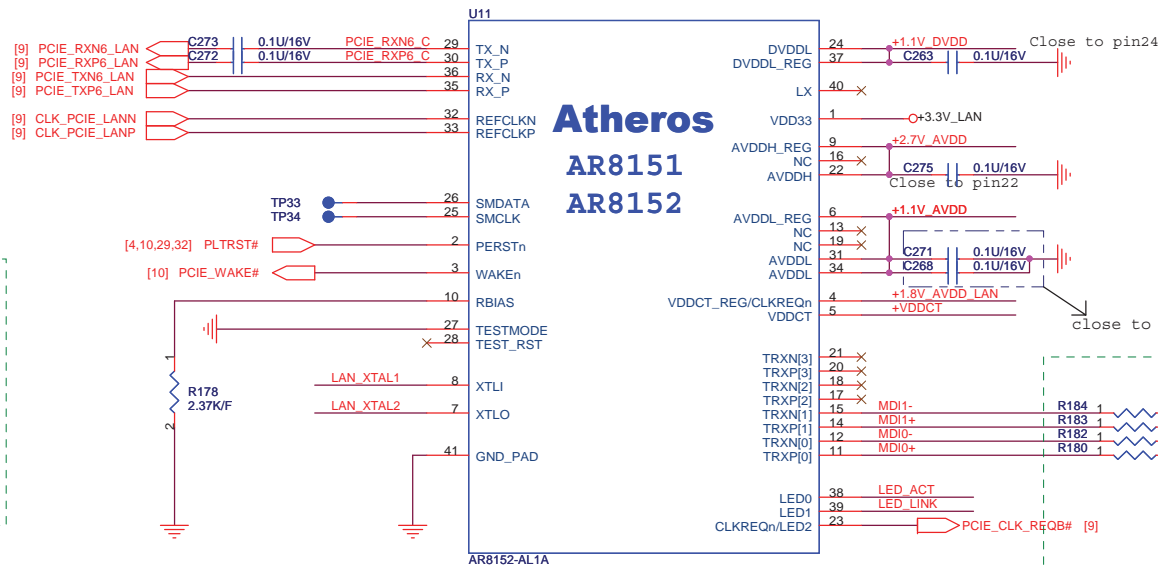
LDO MODE

PWR-ON-STRAPPING

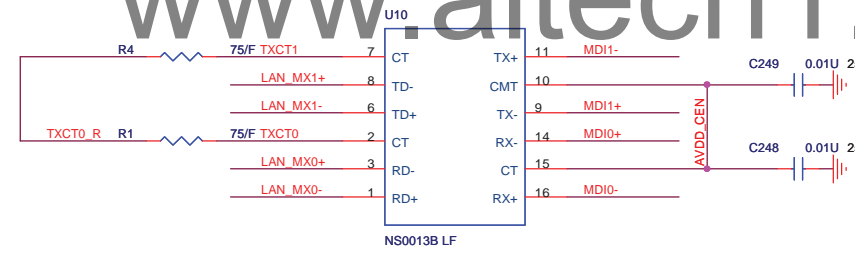
	SWR	LDO
LED_LINK	1	0
LED_ACT	O/C	NO/C
	1	0



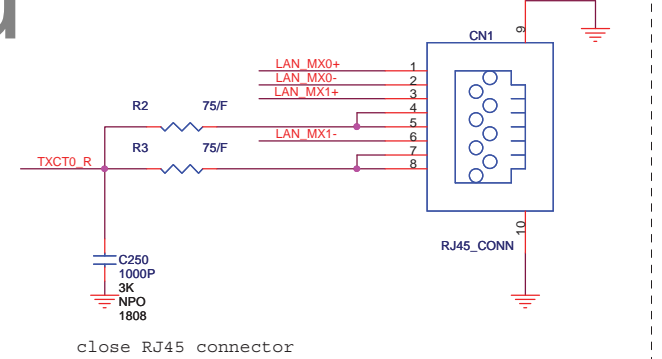
These Caps close LAN Chip VDD33 pins



TRANSFORMER



RJ45



close RJ45 connector



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PROJECT : UM7 UMA

LAN(AR8152/RJ-45)

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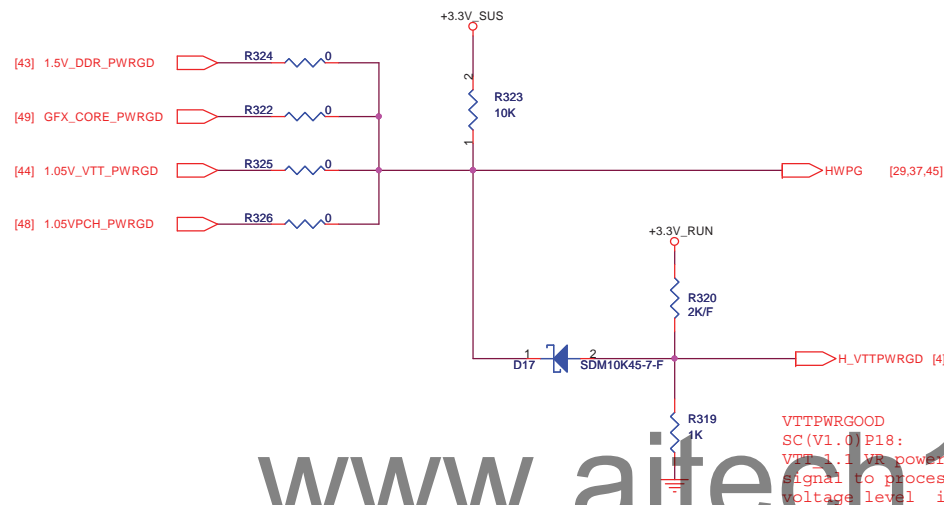
<http://hobi-elektronika.net>



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**PROJECT : UM7 UMA**

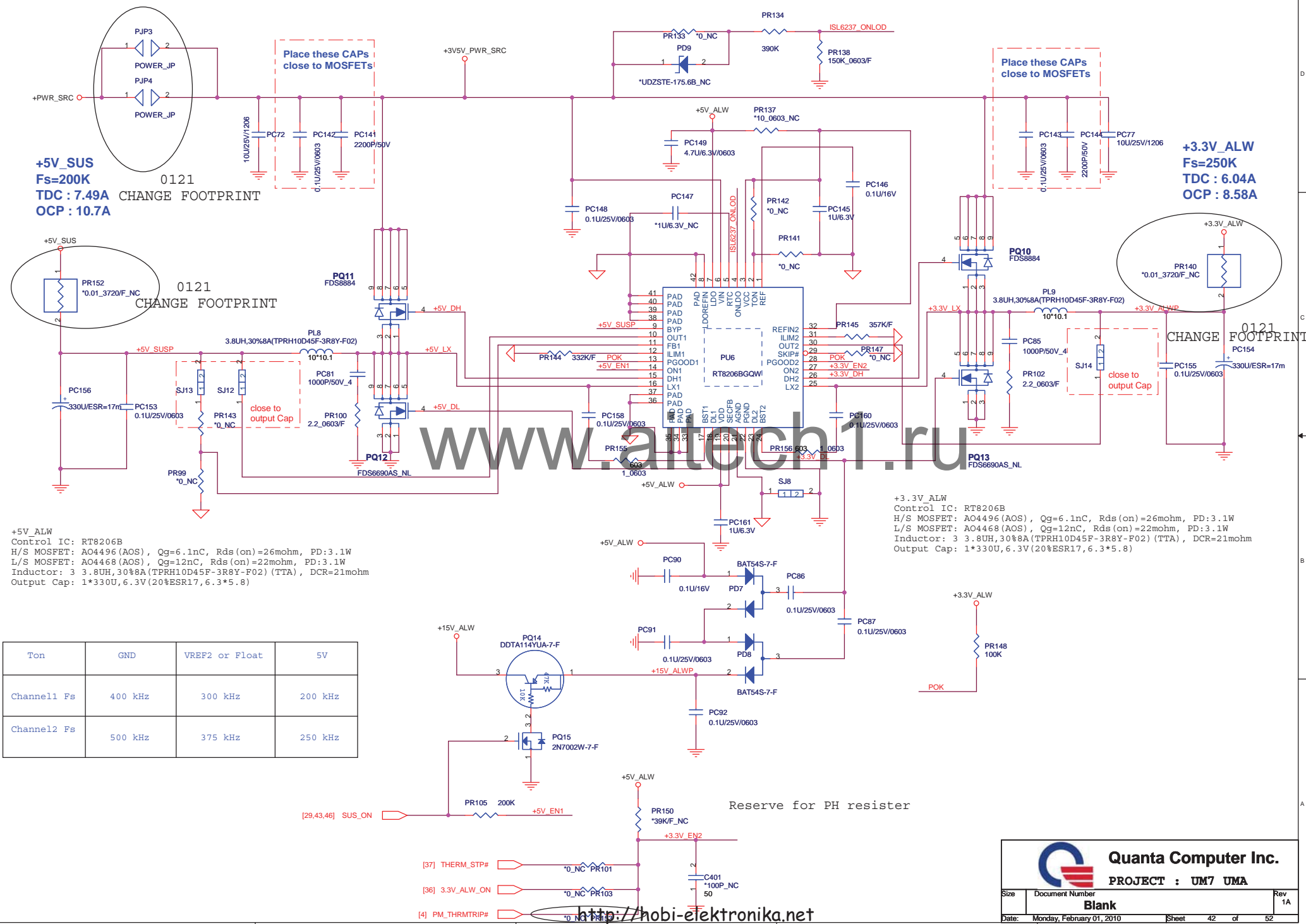
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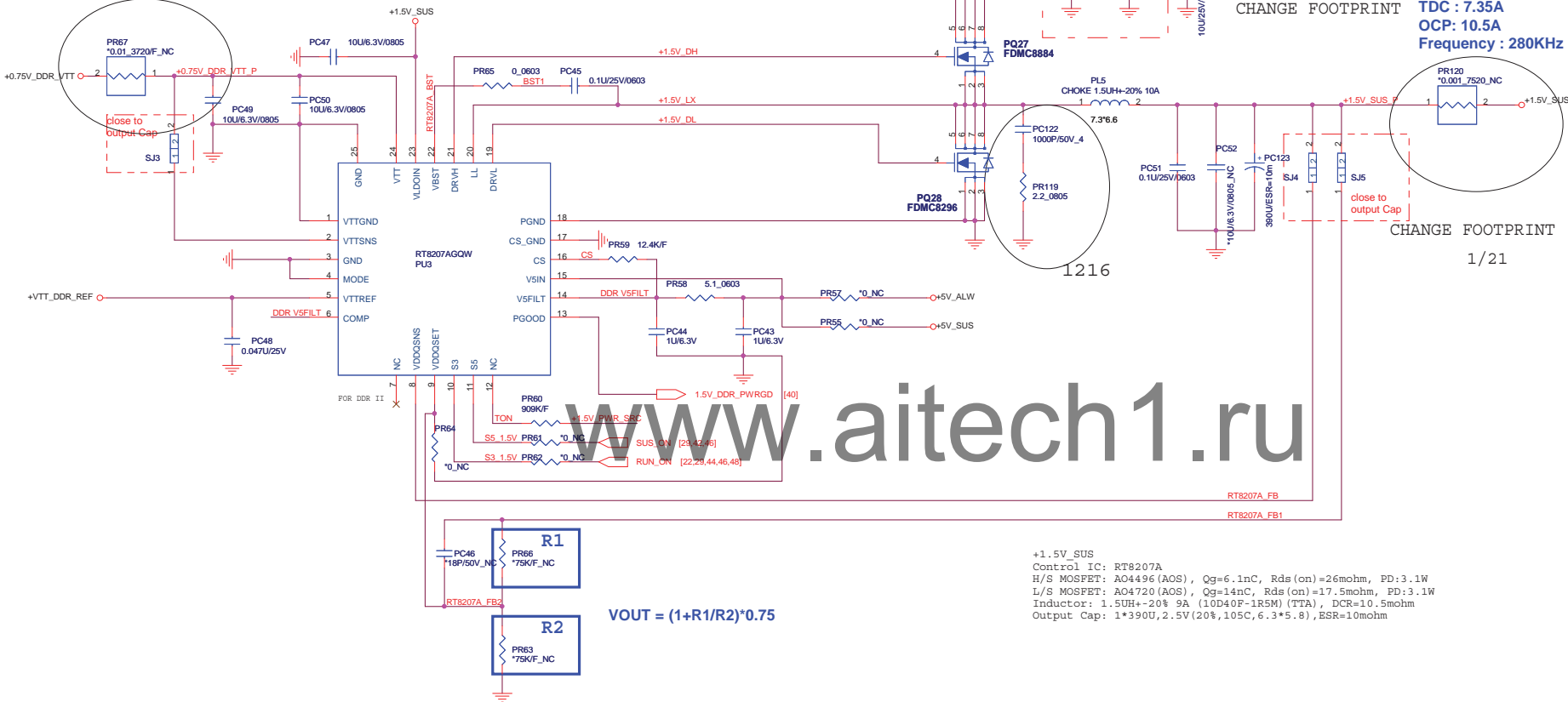
**Quanta Computer Inc.**  
PROJECT : UM7 UMA

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CHANGE FOOTPRINT

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$$VOUT = (1 + R1/R2) * 0.75$$

+1.5V\_SUS  
Control IC: RT8207A  
H/S MOSFET: AO4496 (AOS), Qg=6.1nC, Rds(on)=26mohm, PD:3.1W  
L/S MOSFET: AO4720 (AOS), Qg=14nC, Rds(on)=17.5mohm, PD:3.1W  
Inductor: 1.5uH+-20% 9A (10D40F-1R5M) (TTA), DCR=10.5mohm  
Output Cap: 1\*390U, 2.5V (20%, 105C, 6.3\*5.8), ESR=10mohm

VDDQ and VTT discharge control

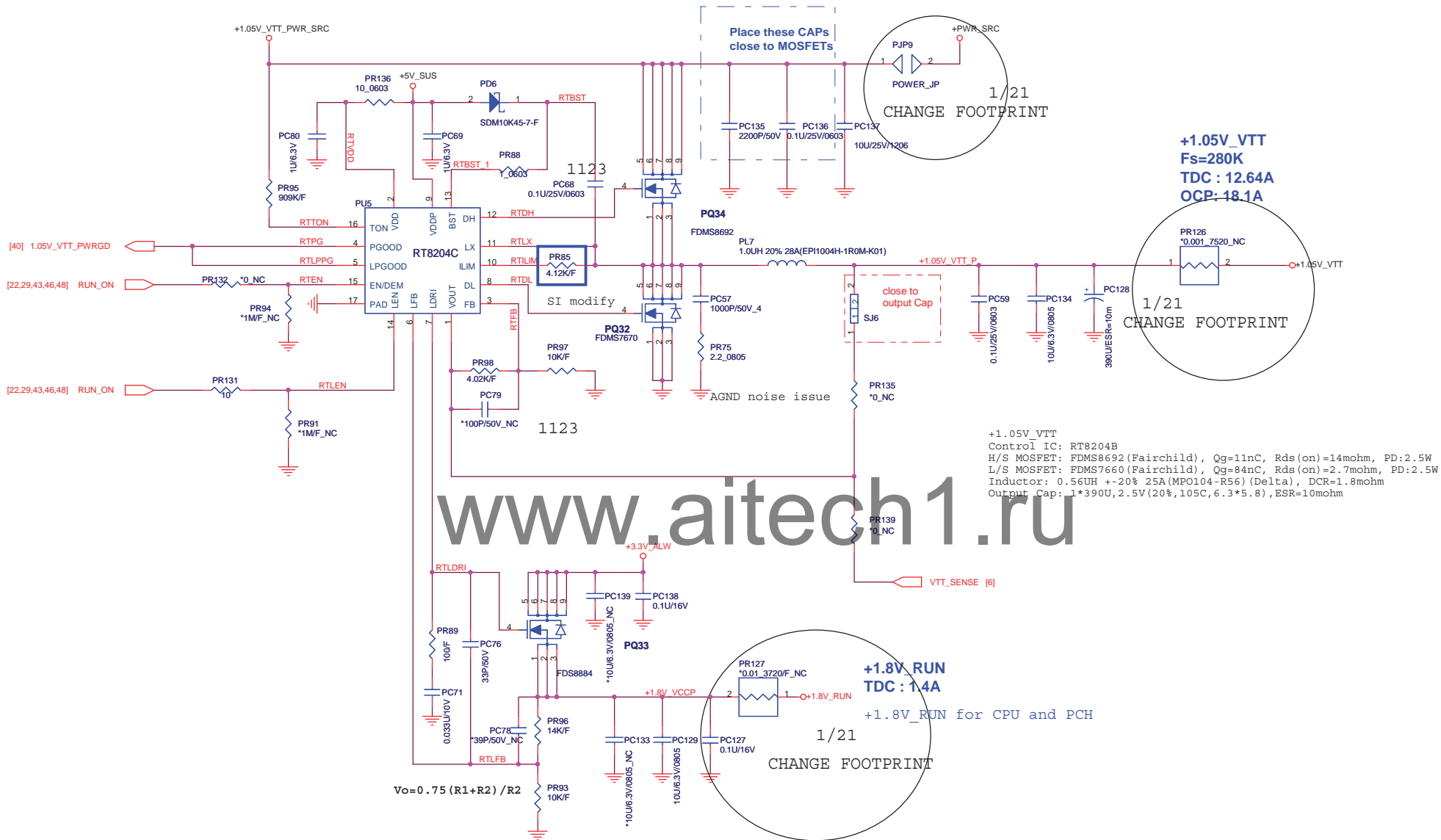
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

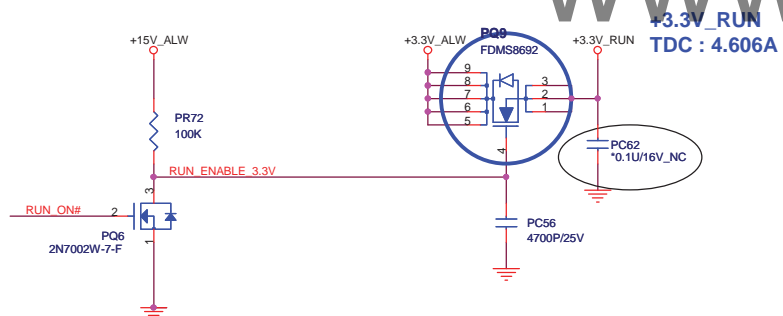
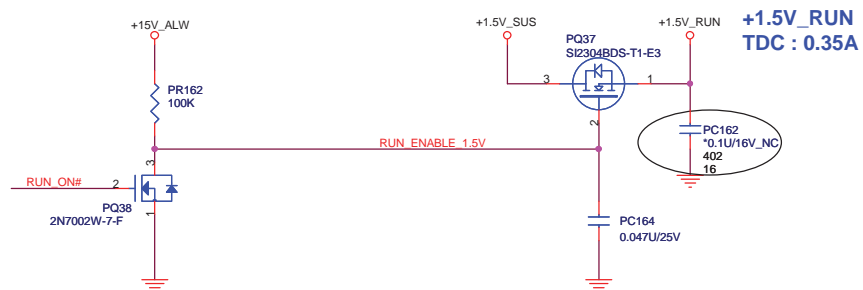
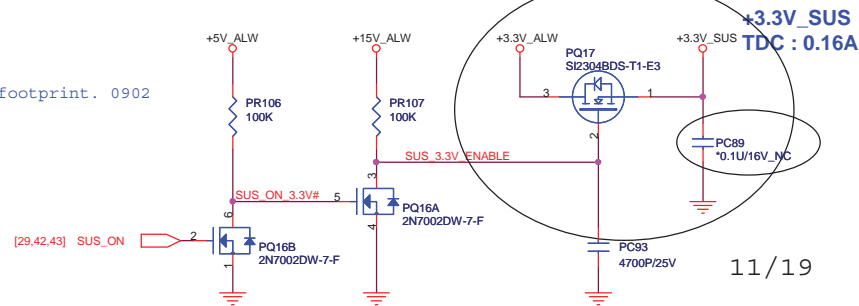
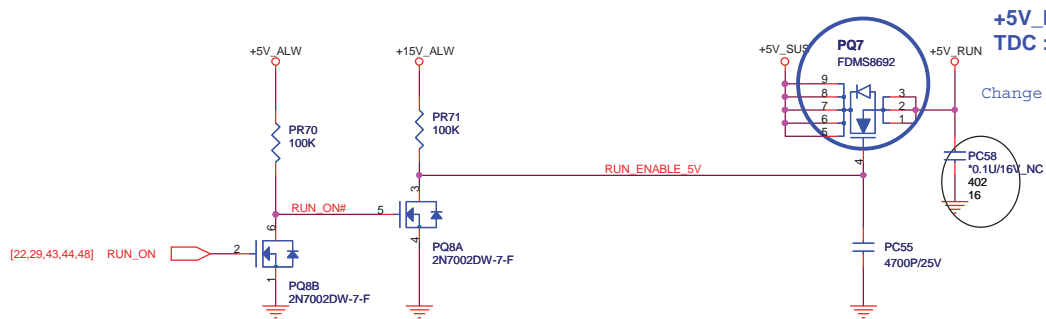
Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

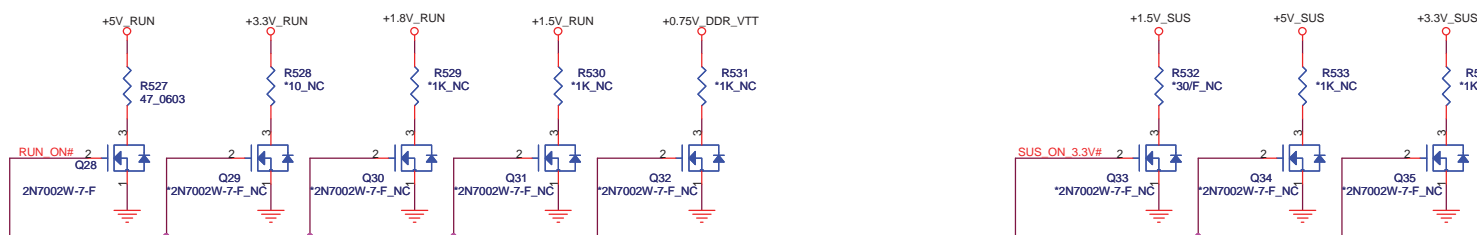


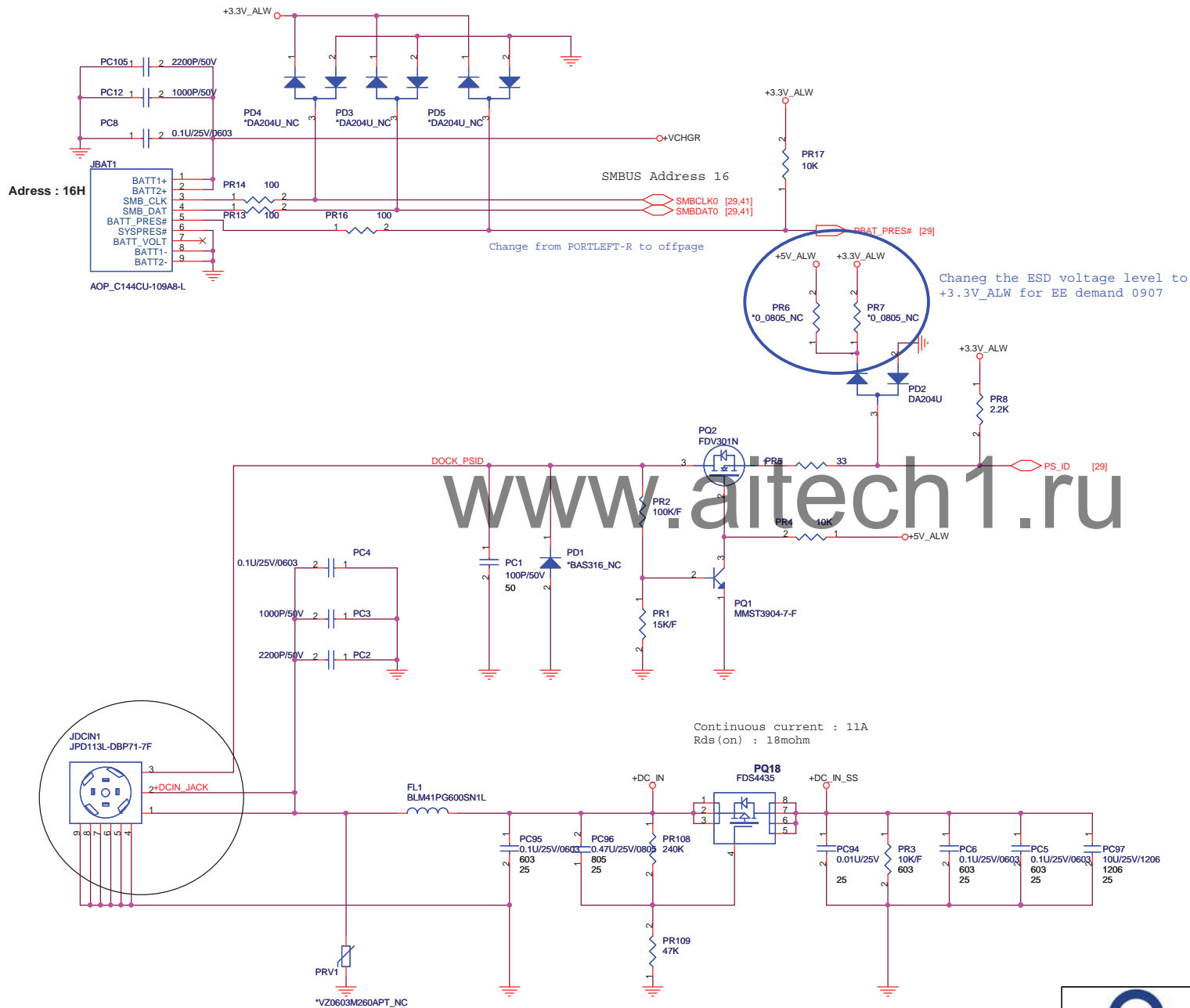
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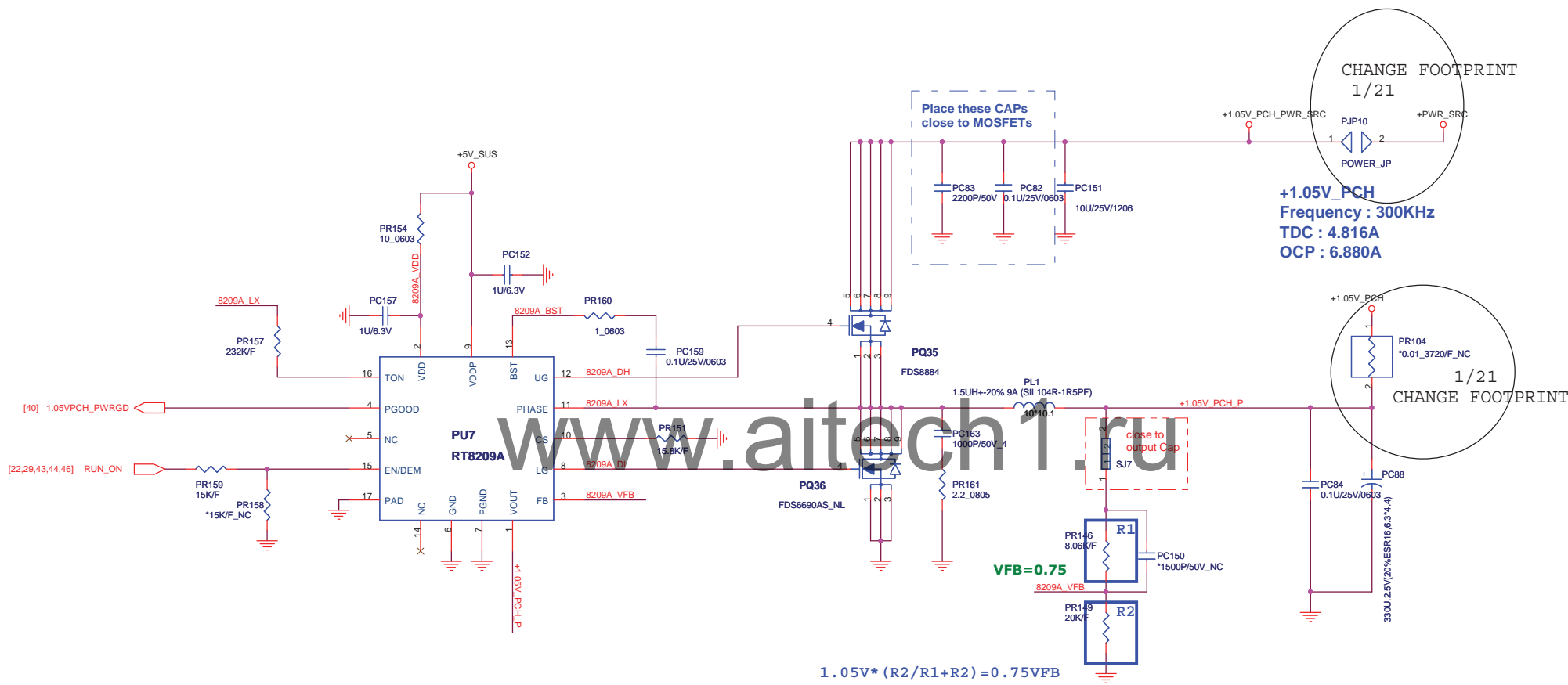




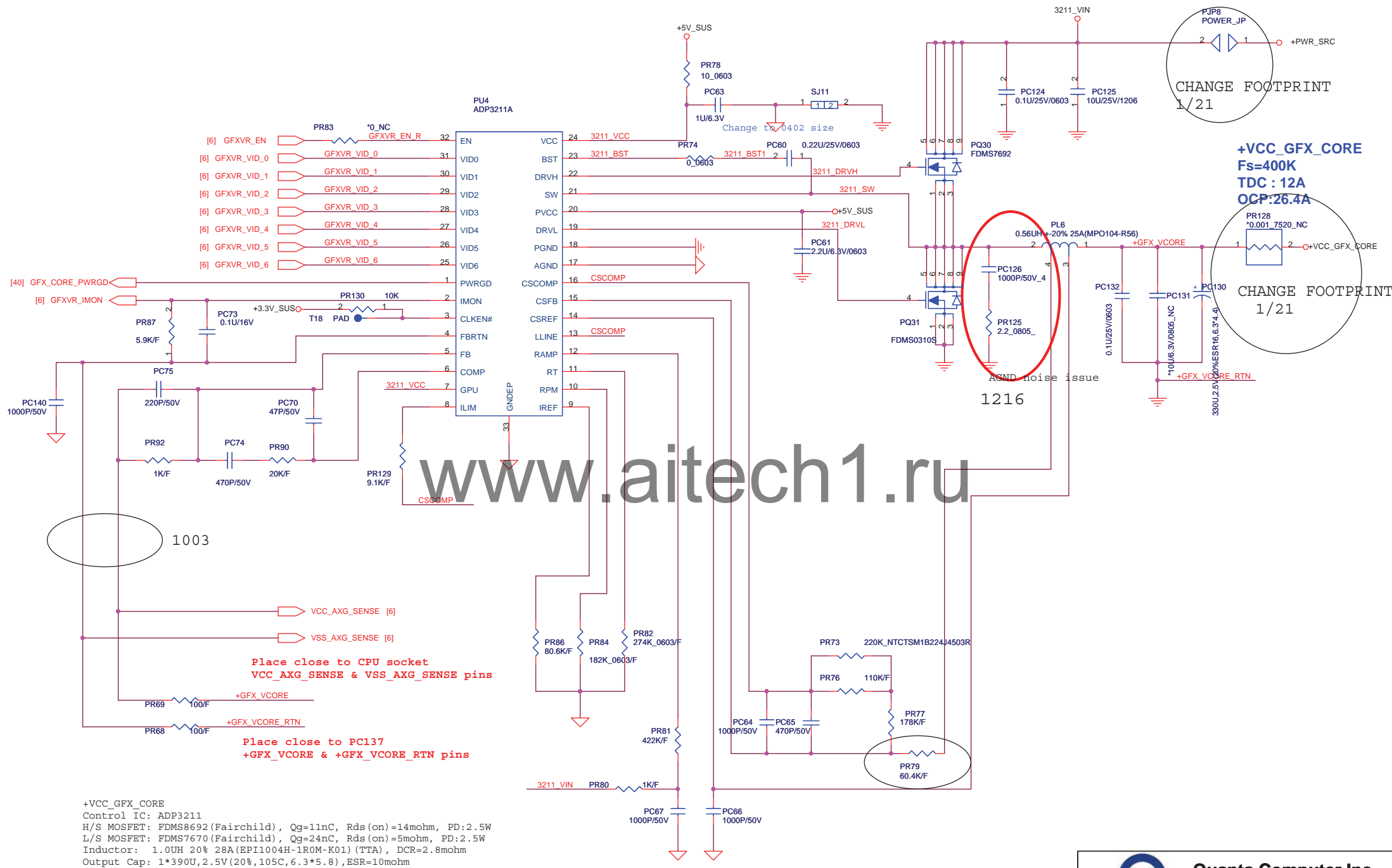
### Reserve discharge path



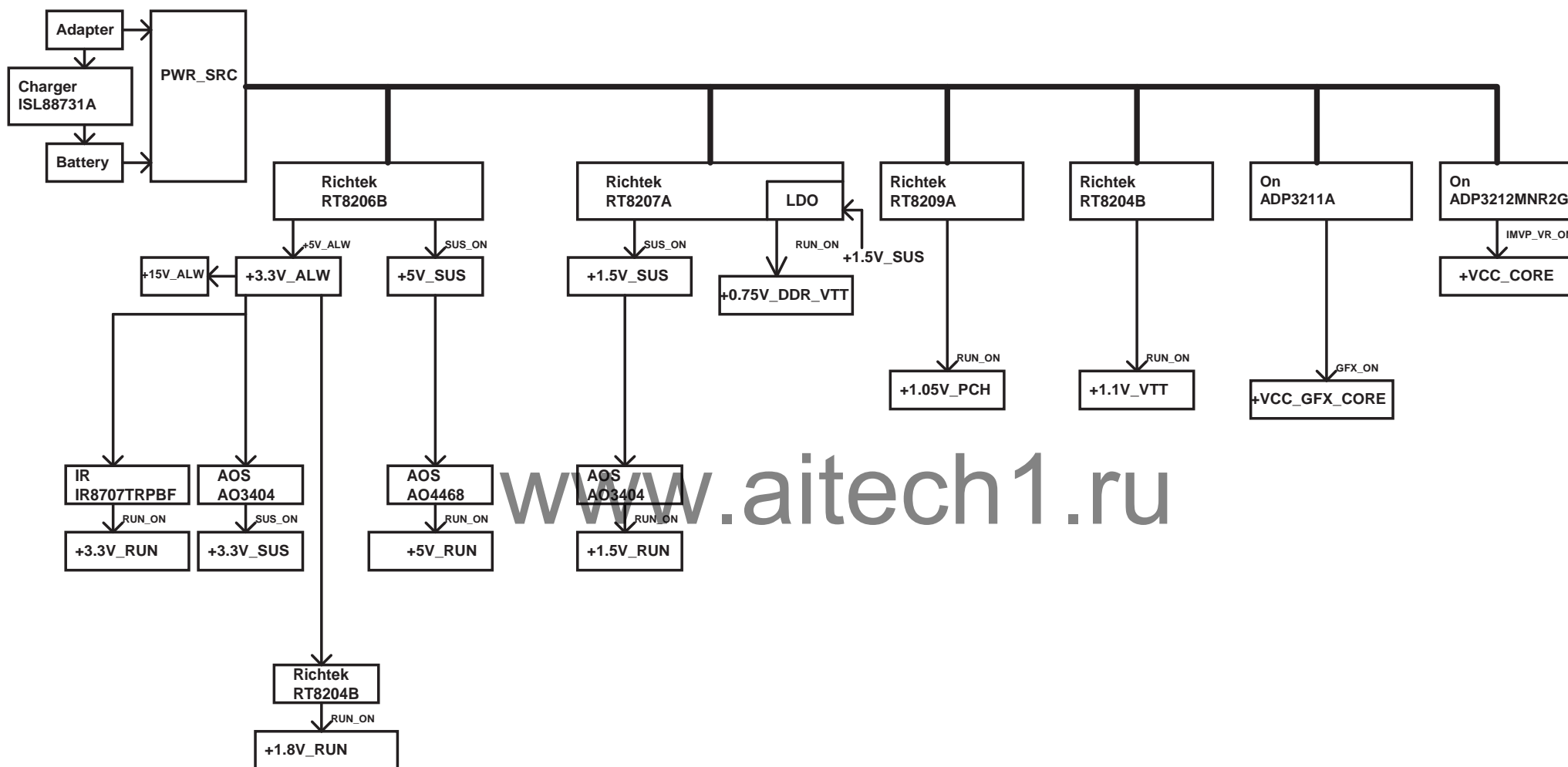








+VCC\_GFX\_CORE  
Control IC: ADP3211  
H/S MOSFET: FDMS8692 (Fairchild),  $Q_g=11nC$ ,  $R_{ds(on)}=14m\Omega$ ,  $P_D=2.5W$   
L/S MOSFET: FDMS7670 (Fairchild),  $Q_g=24nC$ ,  $R_{ds(on)}=5m\Omega$ ,  $P_D=2.5W$   
Inductor: 1.0UH 20% 28A (EPI1004H-1R0M-K01) (TTA),  $DCR=2.8m\Omega$   
Output Cap: 1\*390U, 2.5V (20%, 105C, 6.3\*5.8),  $ESR=10m\Omega$



## Power Design Block Diagram 2009/08/24

